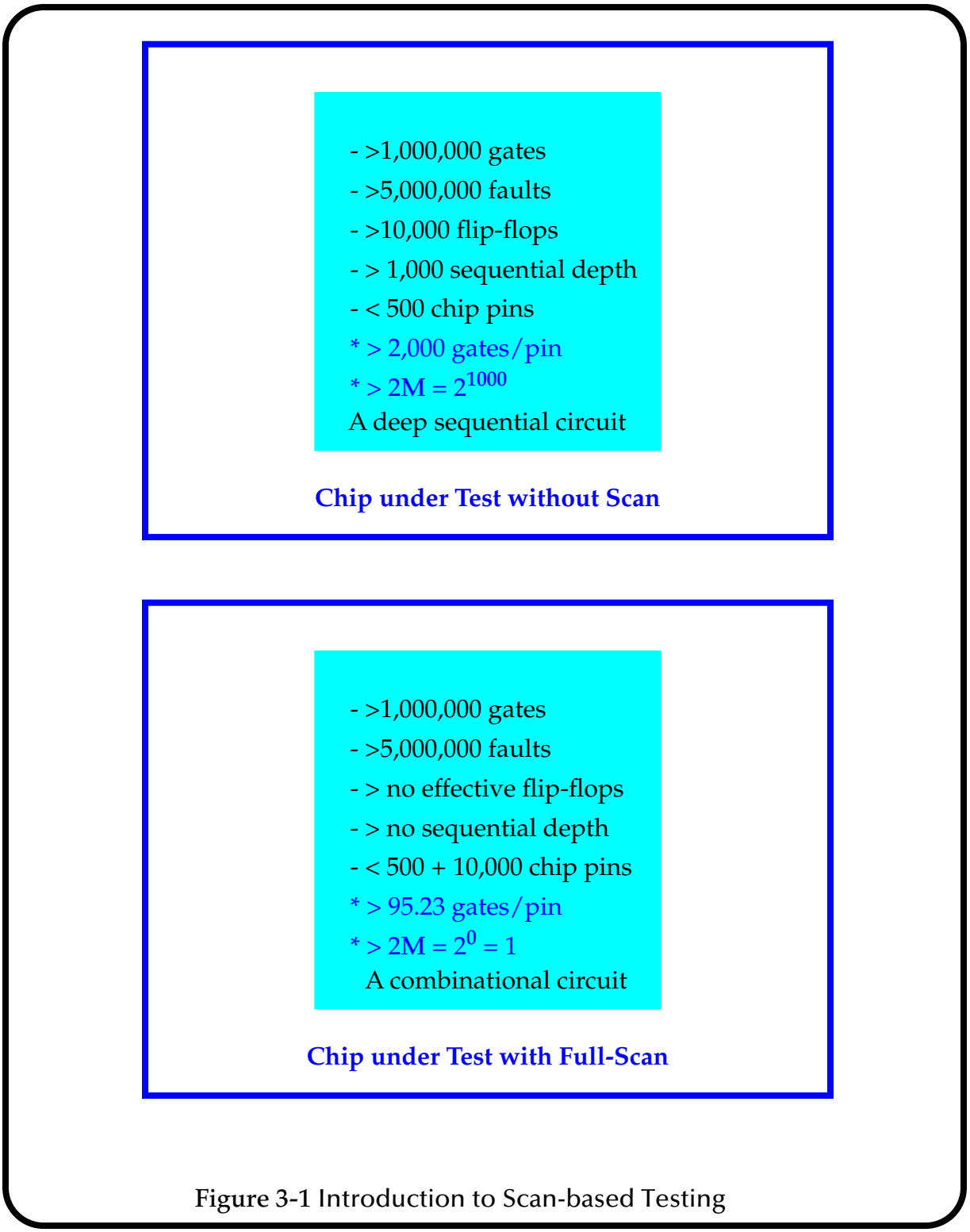


Figure 3-1 Introduction to Scan-based Testing

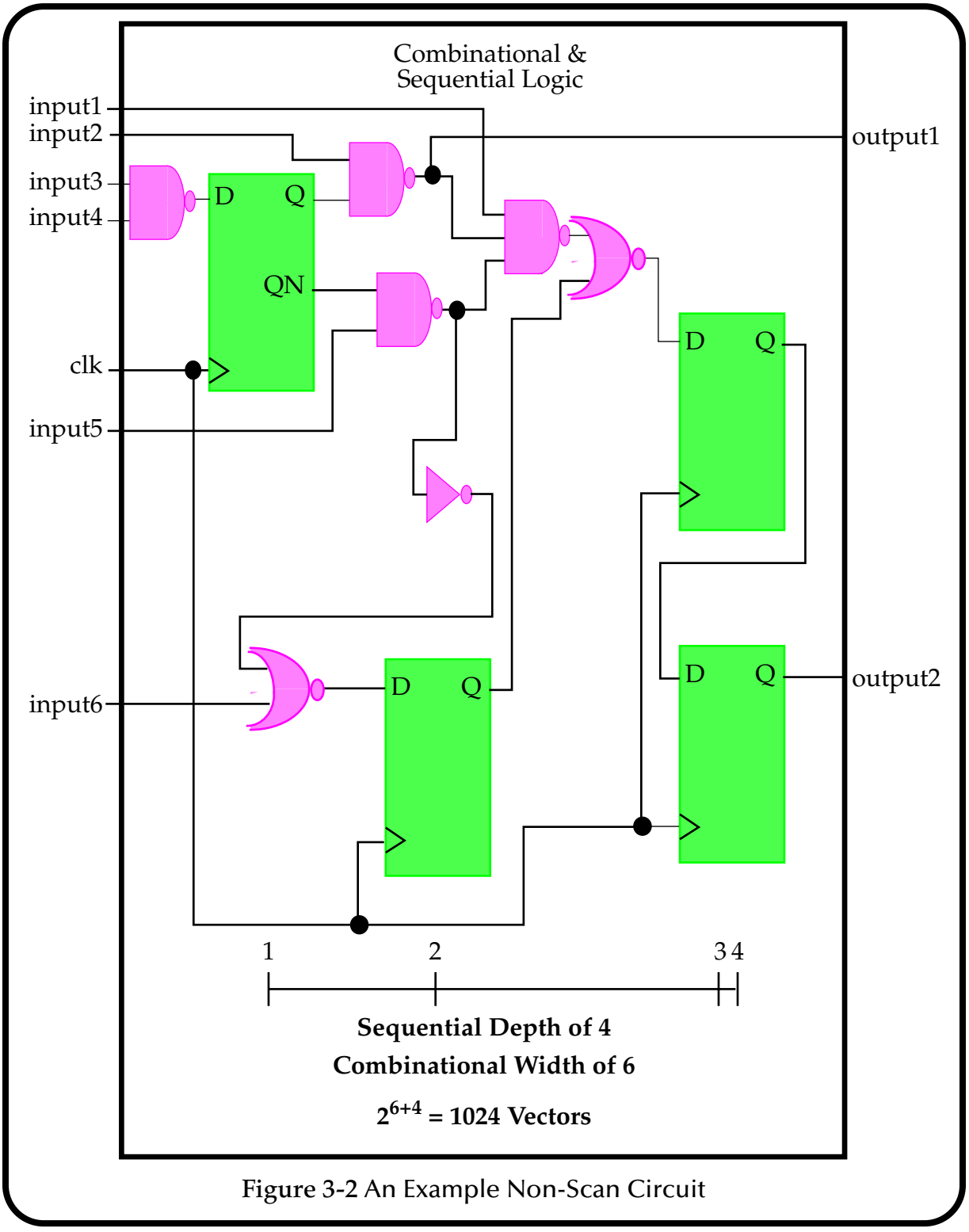


Figure 3-2 An Example Non-Scan Circuit

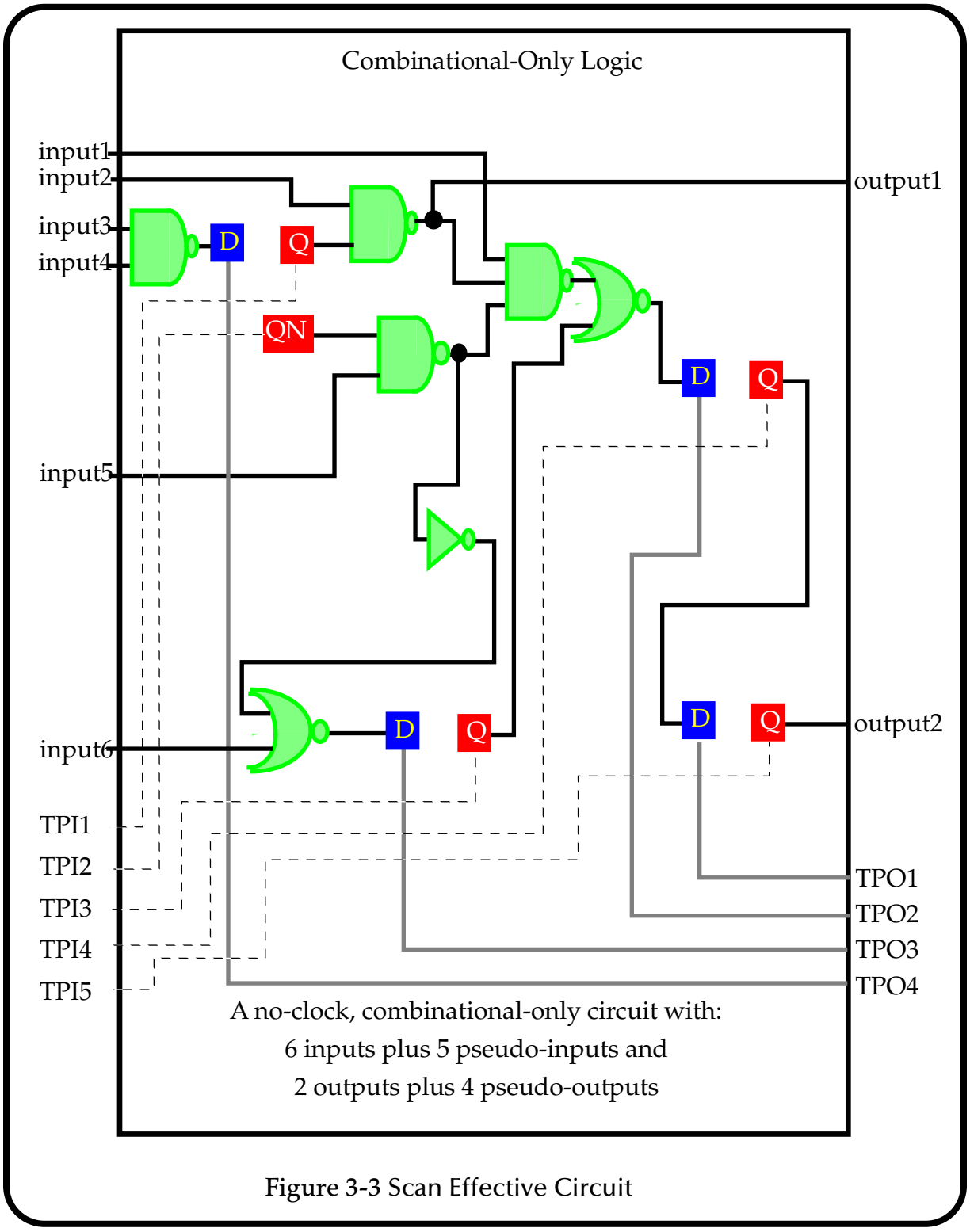


Figure 3-3 Scan Effective Circuit

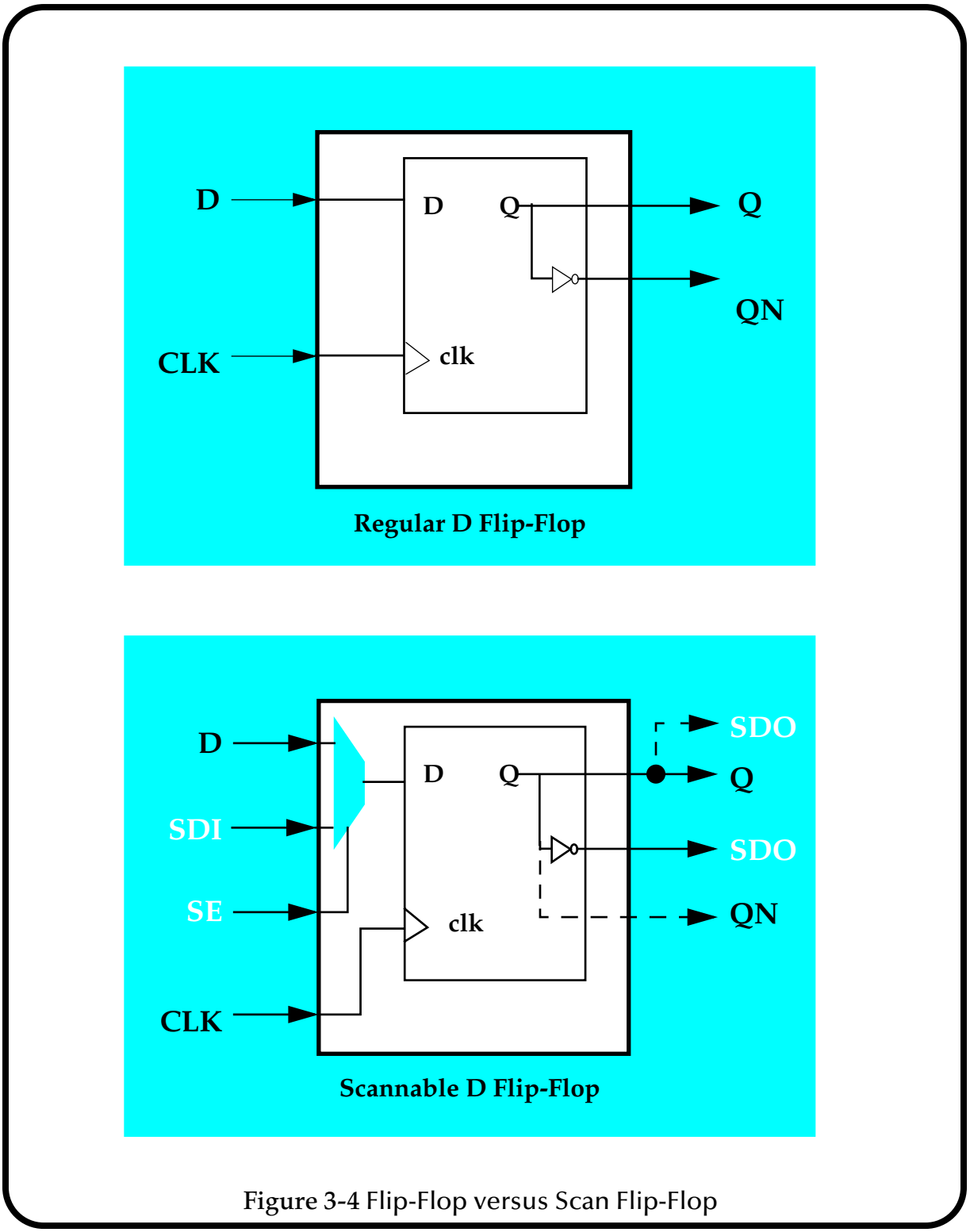
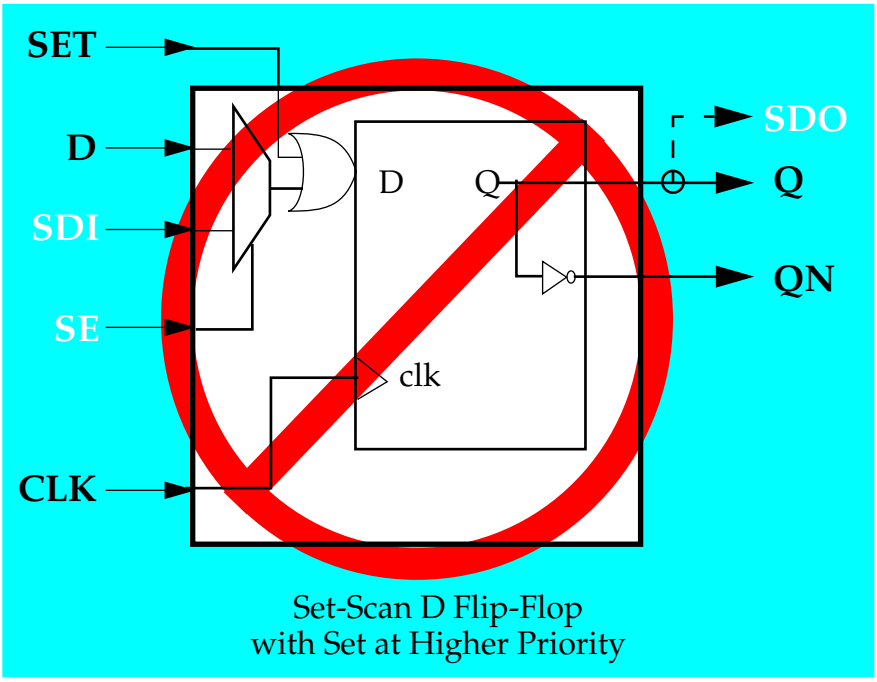
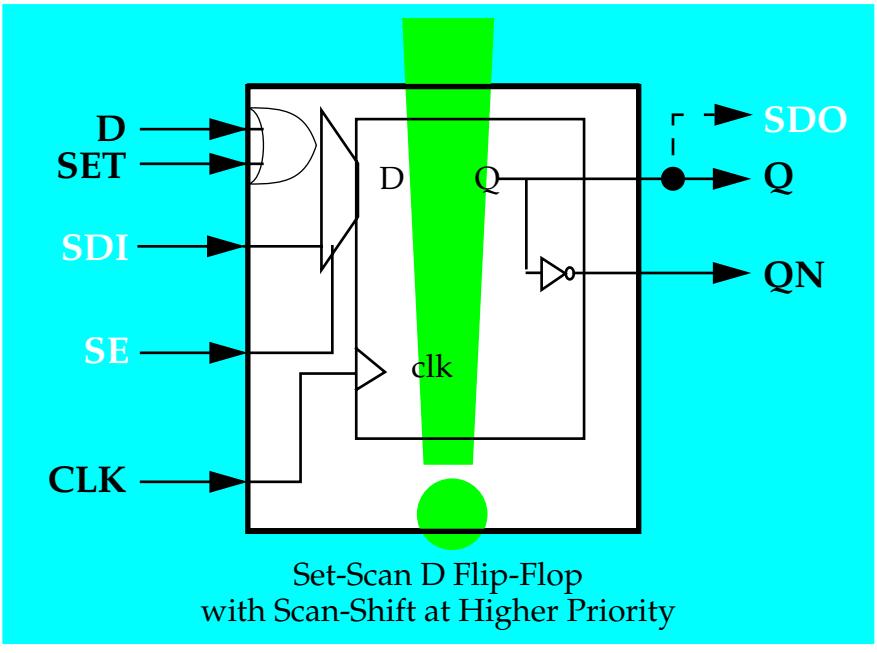


Figure 3-4 Flip-Flop versus Scan Flip-Flop



Set-Scan D Flip-Flop
with Set at Higher Priority



Set-Scan D Flip-Flop
with Scan-Shift at Higher Priority

Figure 3-5 Example Set-Scan Flip-Flops

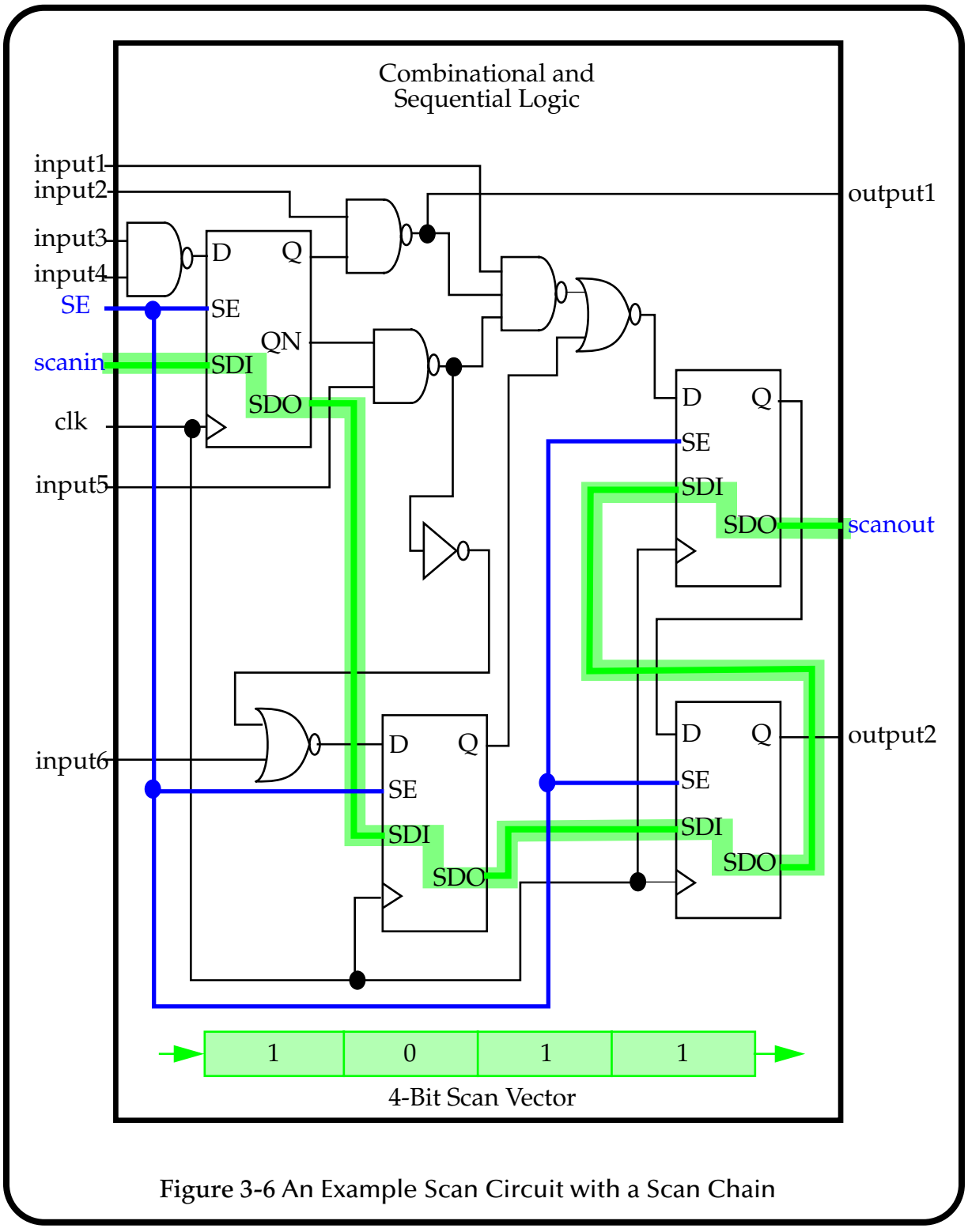
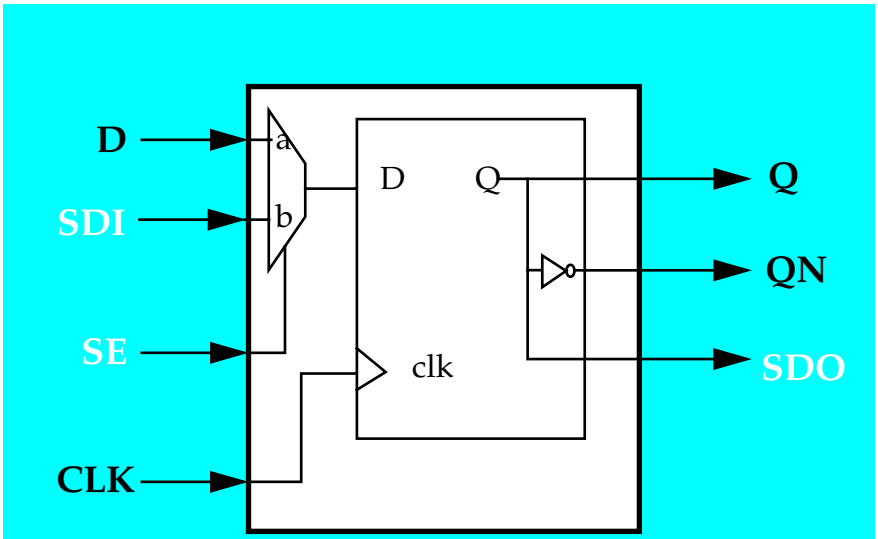


Figure 3-6 An Example Scan Circuit with a Scan Chain



Scannable D Flip-Flop

The scan cell provides observability and controllability of the signal path by conducting the four transfer functions of a scan element.

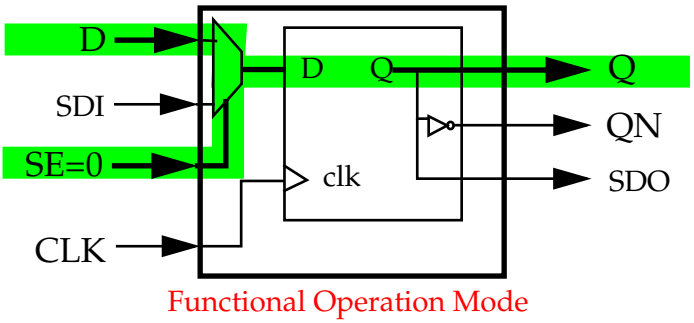
Operate: D to Q through port a of the input multiplexer: allows normal transparent operation of the element.

Scan Sample: D to SDO through port a of the input multiplexer: gives observability of logic that fans into the scan element.

Scan Load/Shift: SDI to SDO through the b port of the multiplexer: used to serially load/shift data into the scan chain while simultaneously unloading the last sample.

Scan Data Apply: SDI to Q through the b port of the multiplexer: allows the scan element to control the value of the output, thereby controlling the logic driven by Q.

Figure 3-7 Scan Element Operations

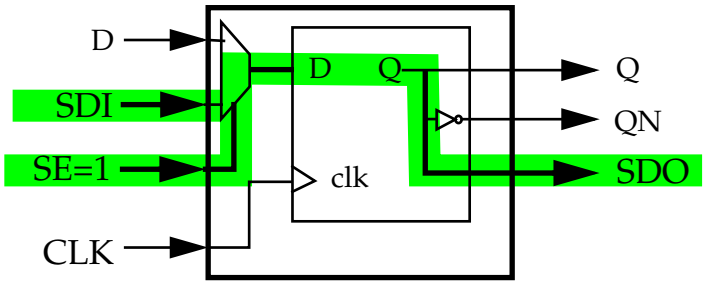


Functional Operation Mode

From normal operation:

While the clock is low, apply test data to SDI and Place SE = 1

At the rising edge of the clock, test data will be loaded

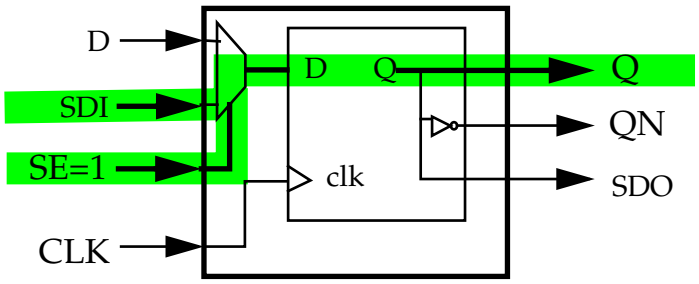


Scan Shift Load/Unload Mode

Apply clocks for scan length

When chain is loaded, the last shift clock will apply scan data

While the clock is low, place SE = 0



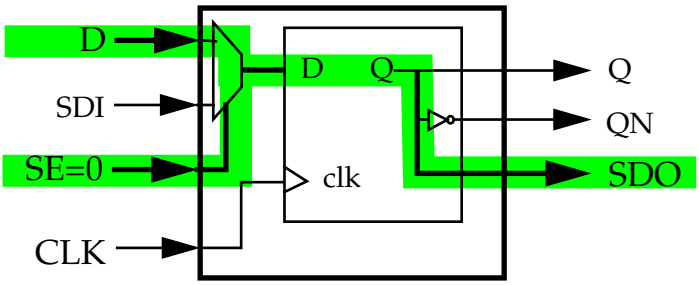
Scan Apply Mode (Last Shift)

Normal circuit response will be applied to D

The next rising edge of the clock will sample D

Return to Load/Shift mode to unload circuit response sample

NOTE: unloading is simultaneous with loading the next test



Scan Sample Mode

Repeat operations until all vectors have been applied

NOTE: the chip's primary inputs must be applied during the scan apply mode (after the last shift)

Figure 3-8 Example Scan Test Sequencing

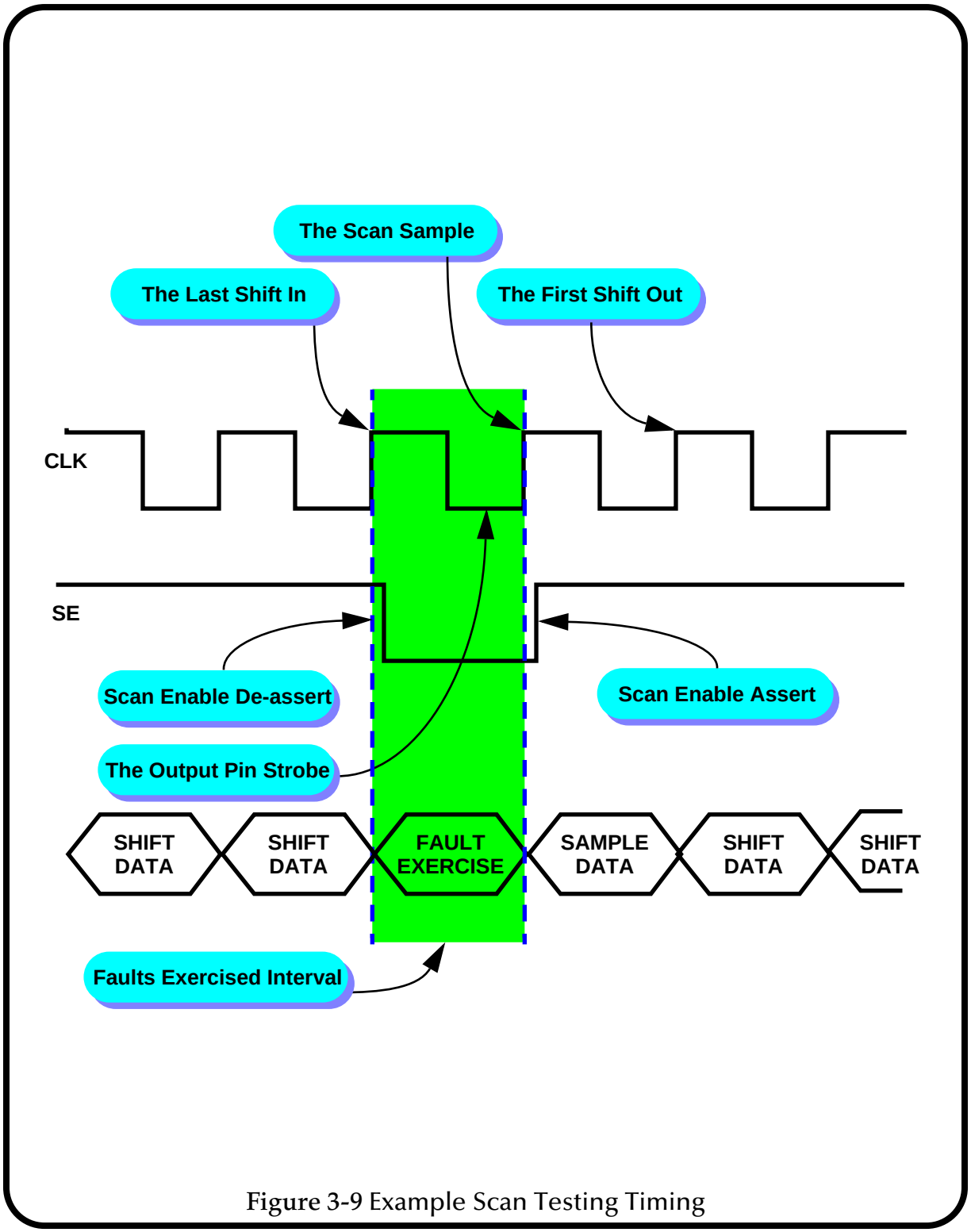


Figure 3-9 Example Scan Testing Timing

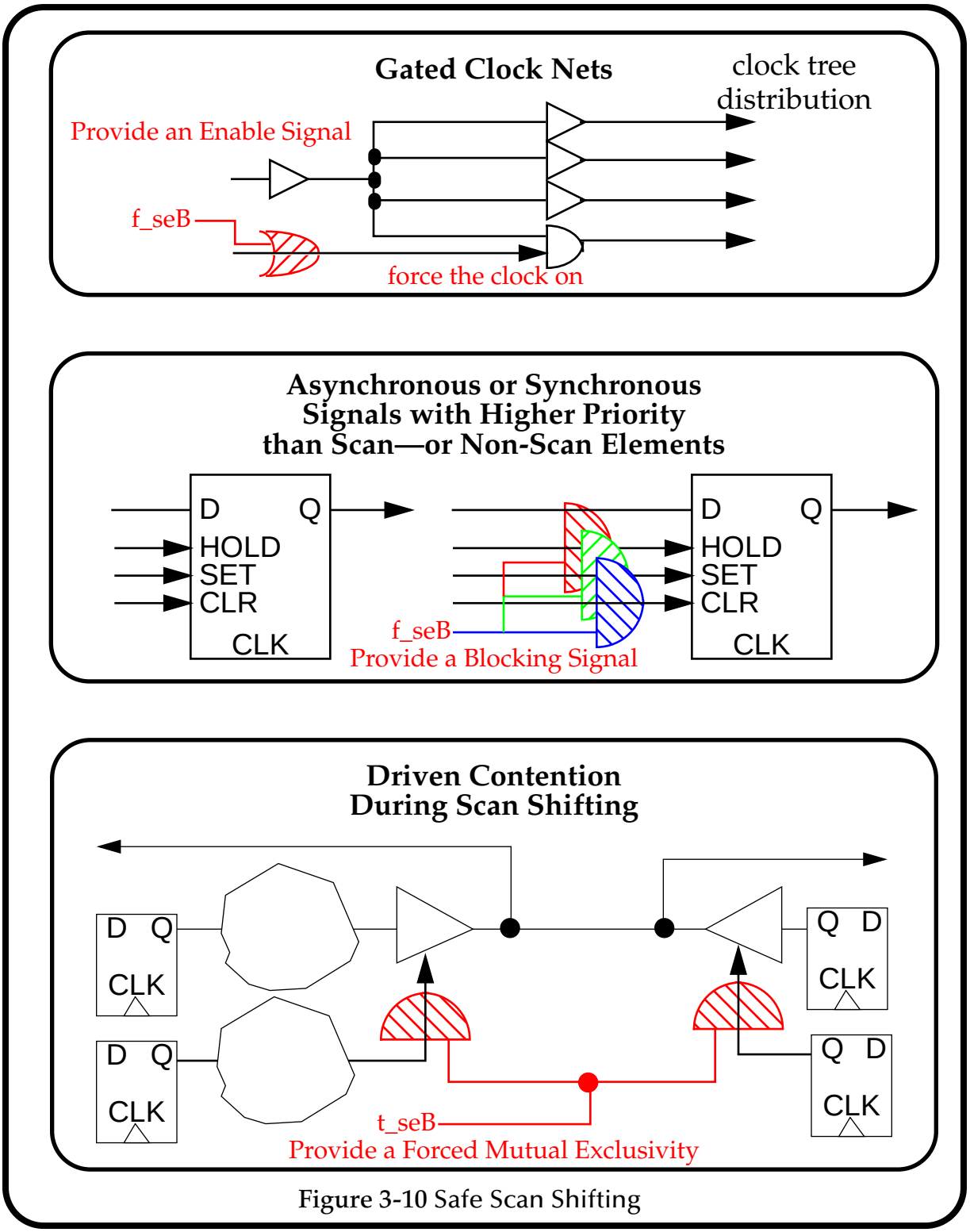


Figure 3-10 Safe Scan Shifting

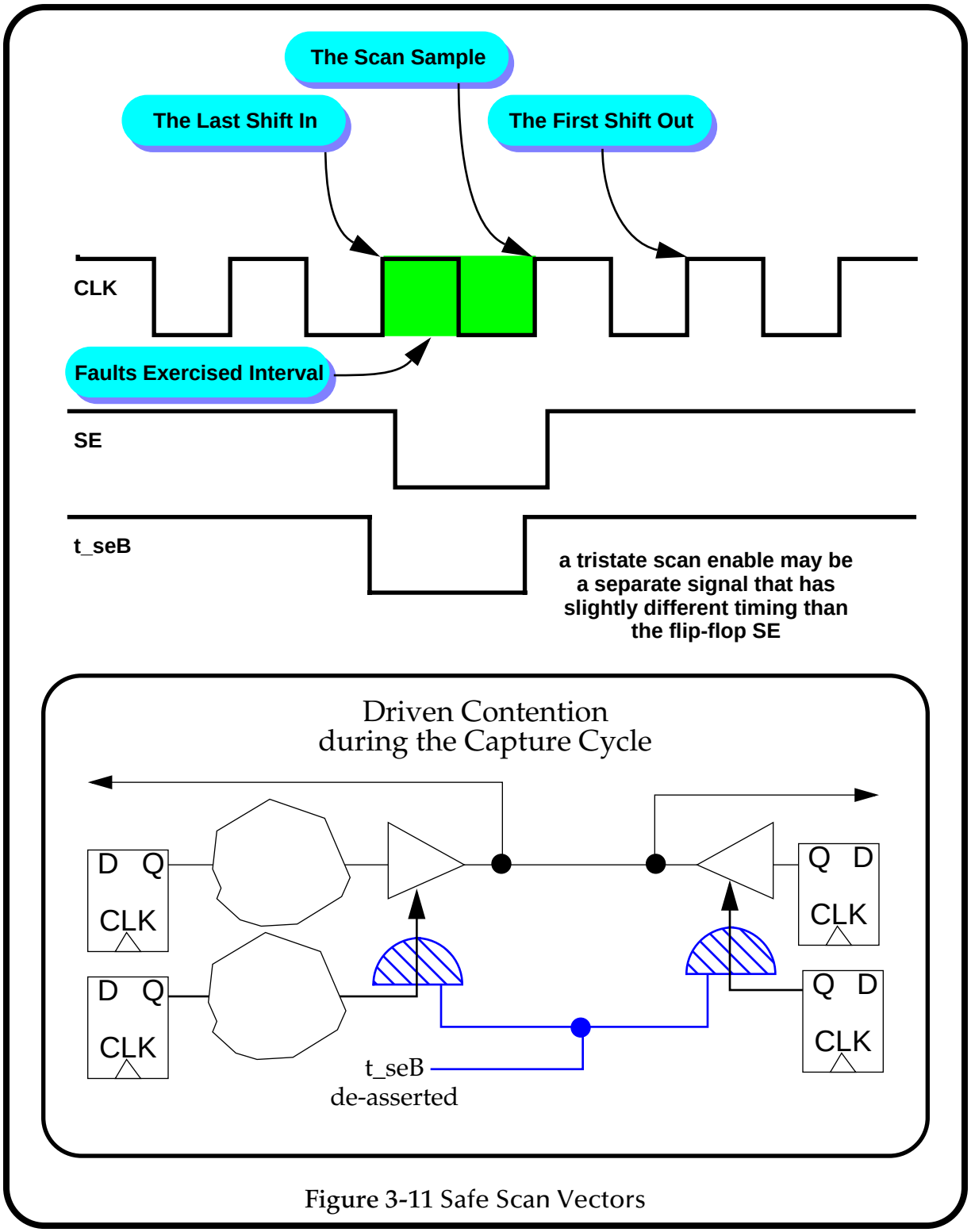


Figure 3-11 Safe Scan Vectors

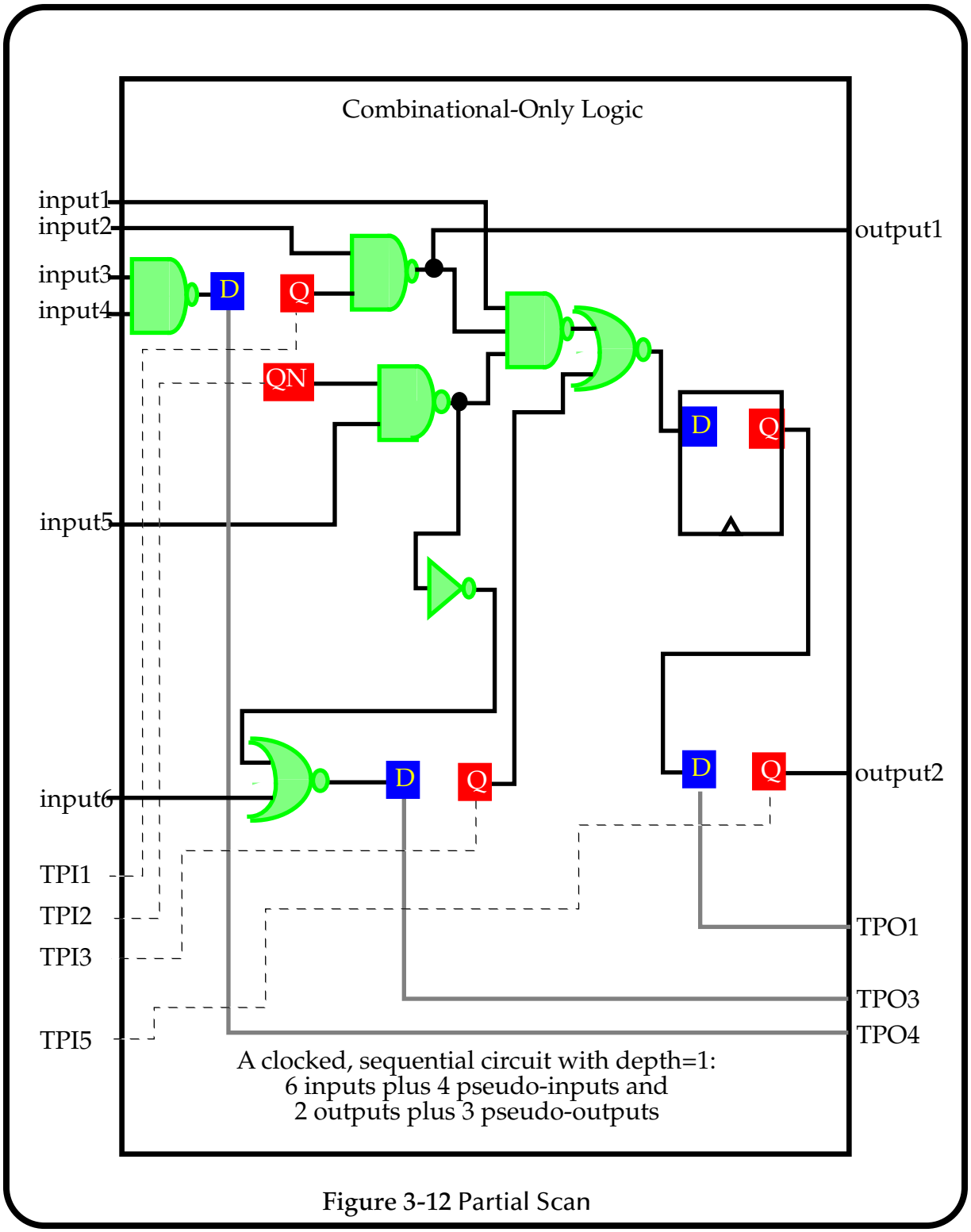


Figure 3-12 Partial Scan

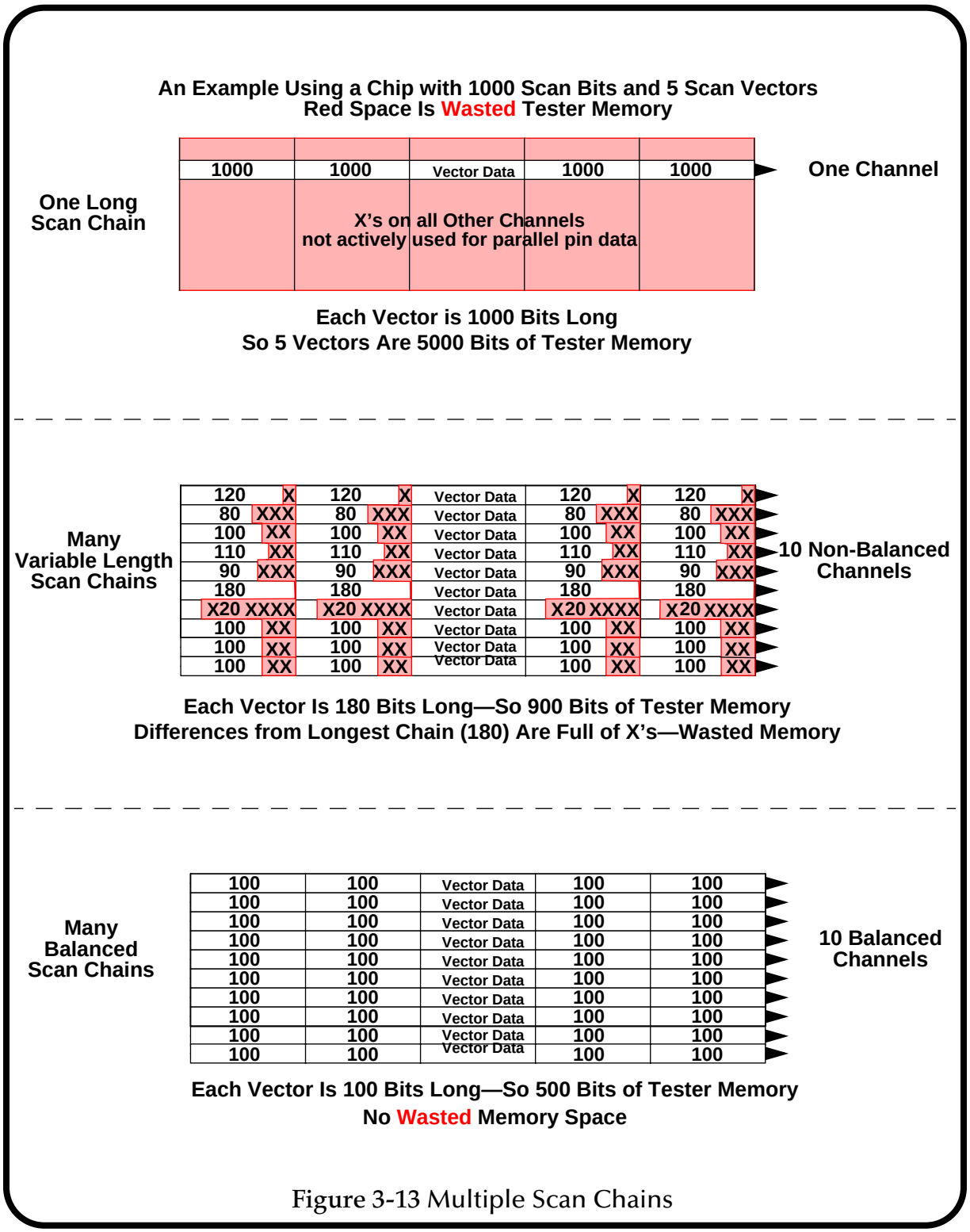


Figure 3-13 Multiple Scan Chains

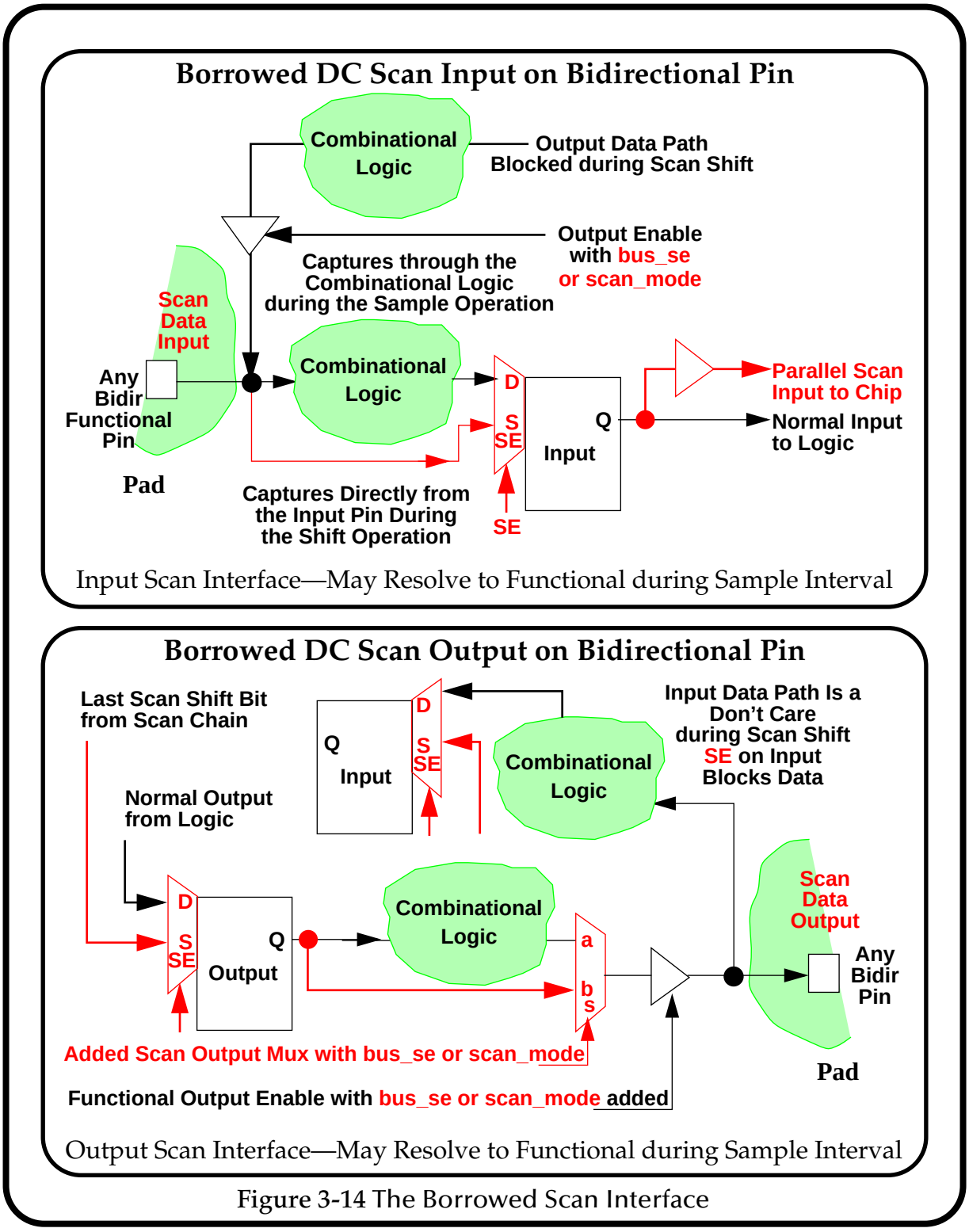


Figure 3-14 The Borrowed Scan Interface

- Scan Bypass Clocks
- Scan Testing an On-Chip Clock Source

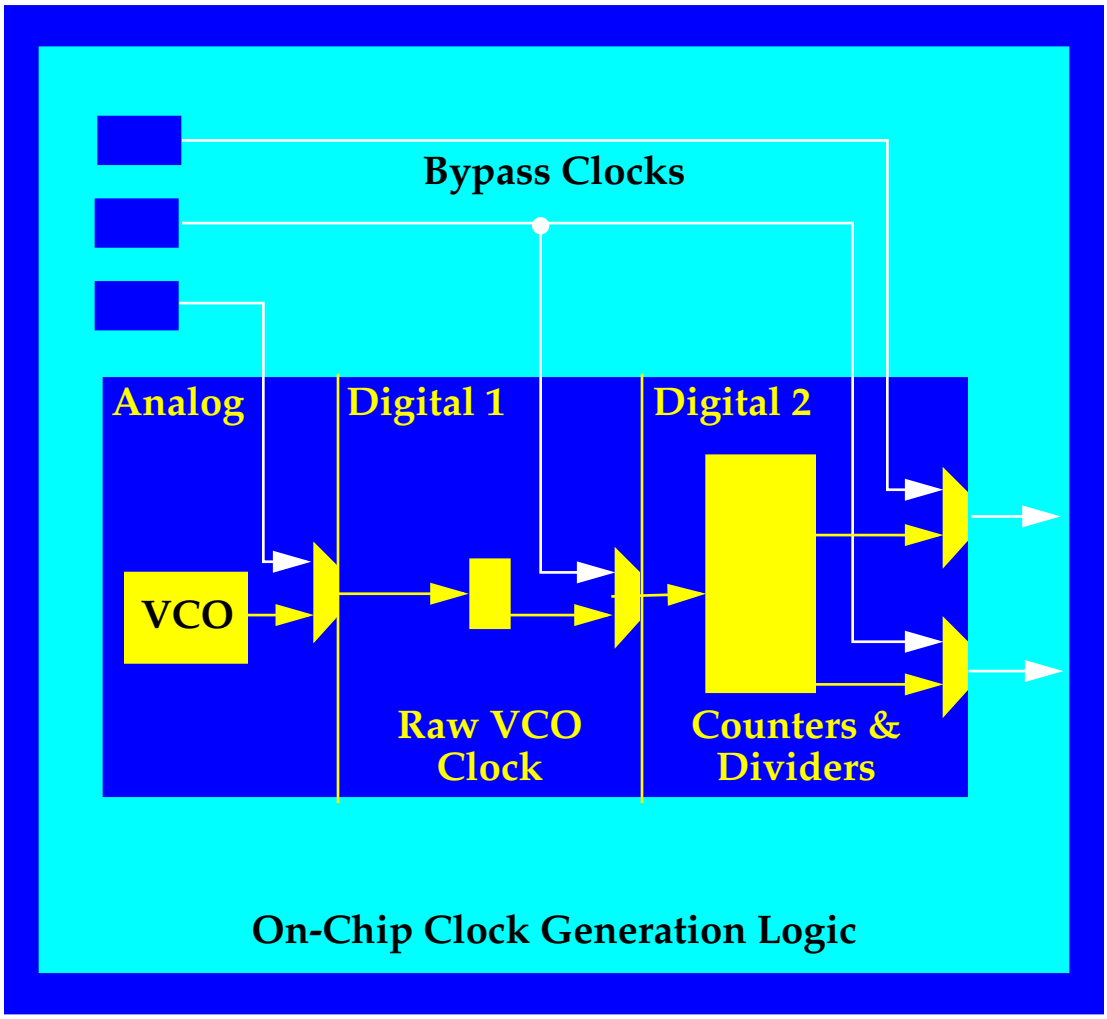


Figure 3-15 Clocking and Scan

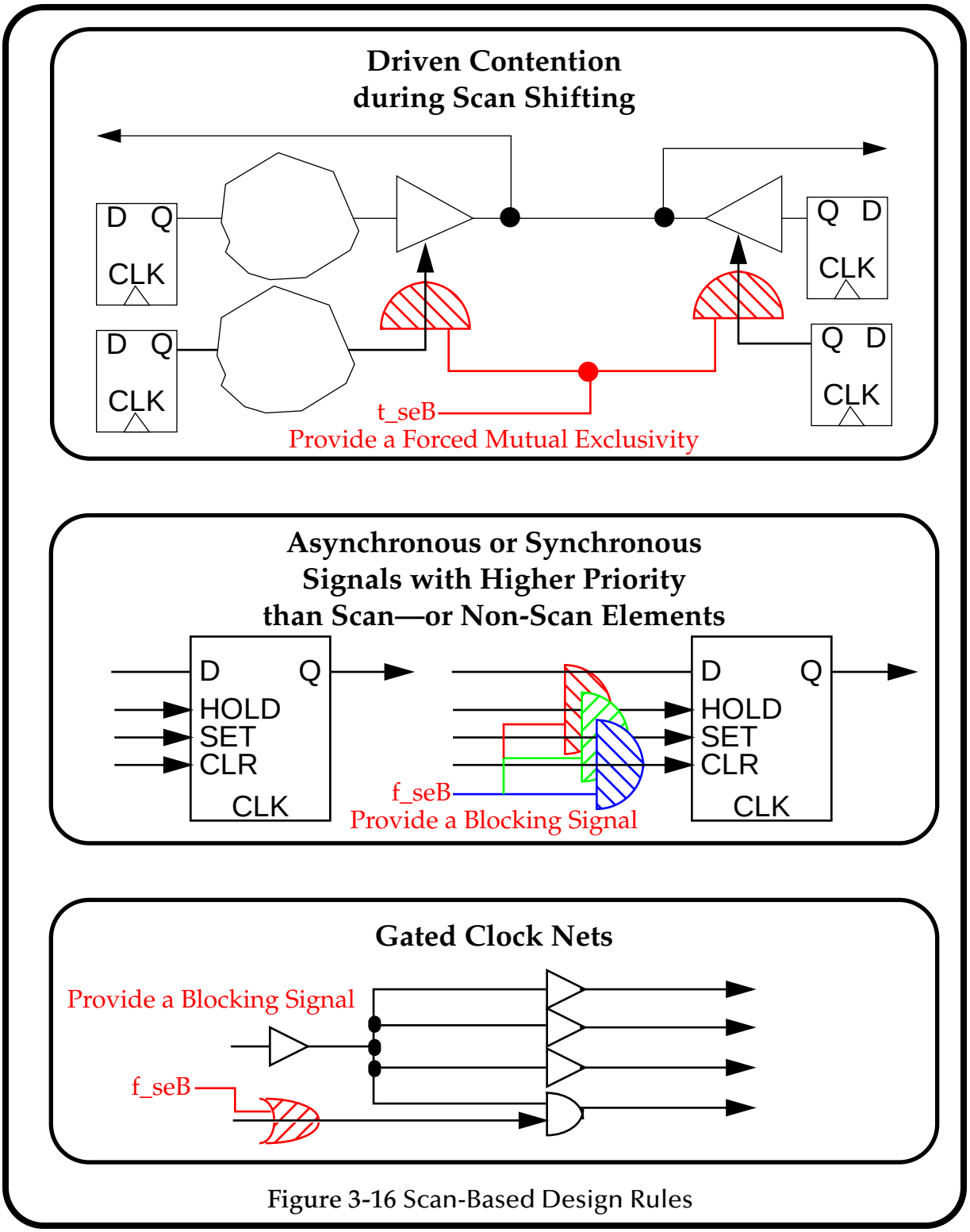


Figure 3-16 Scan-Based Design Rules

Basic Netlist Scan Insertion

- Element Substitution
- Ports, Routing & Connection of SE
- Ports, Routing & Connection of SDI-SDO

Extras

- Tristate "Safe Shift" Logic
- Asynchronous "Safe Shift" Logic
- Gated-Clock "Safe Shift" Logic
- Multiple Scan Chains
- Scan-Bit Re-Ordering

Clock Considerations

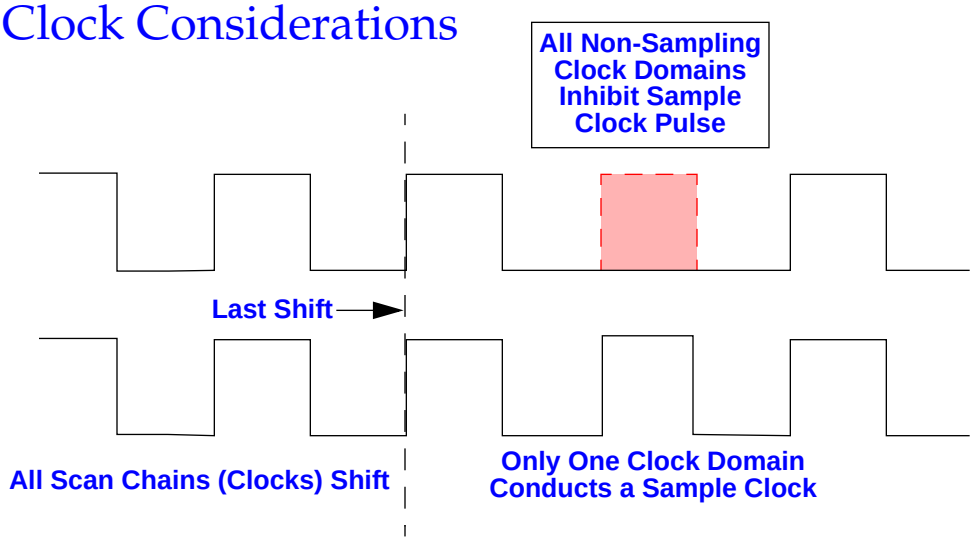


Figure 3-17 DC Scan Insertion

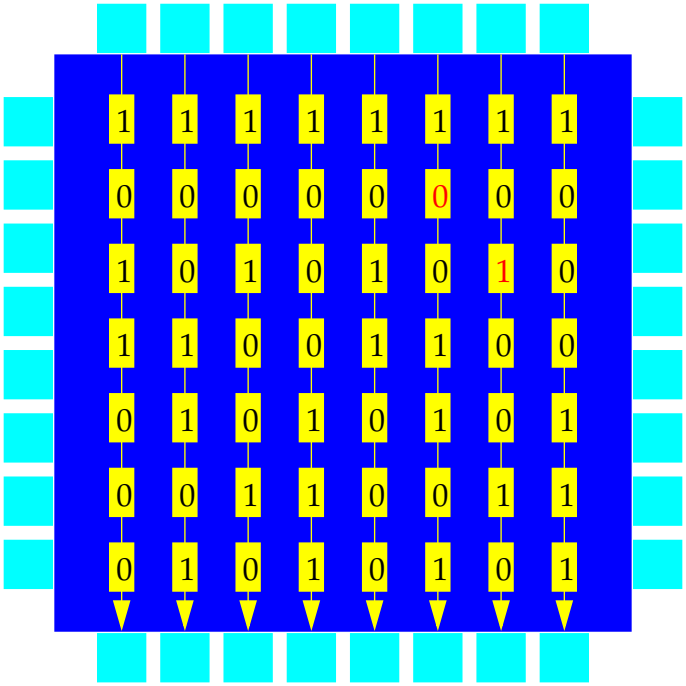


Figure 3-18 Stuck-At Scan Diagnostics

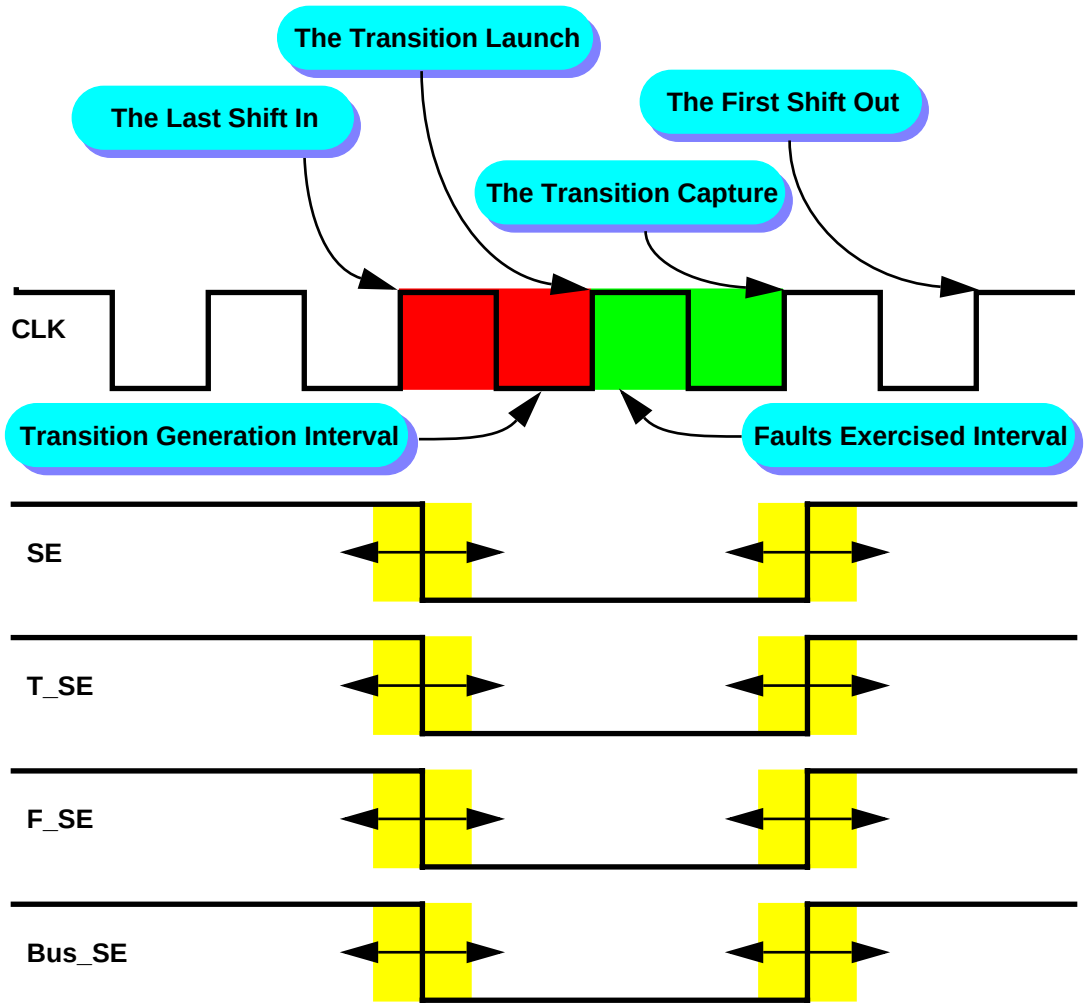
Basic Purpose

- Frequency Assessment
- Pin Specifications
- Delay Fault Content

Cost Drivers

- No Functional Vectors
- Fewer Overall Vectors
- Deterministic Grade

Figure 3-19 At-Speed Scan Goals



Separate Scan Enables for Tristate Drivers, Clock Forcing Functions, Logic Forcing Functions, Scan Interface Forcing Functions, and the Scan Multiplexor Control

Because the Different Elements Have Different Timing Requirements

Figure 3-20 At-Speed Scan Testing

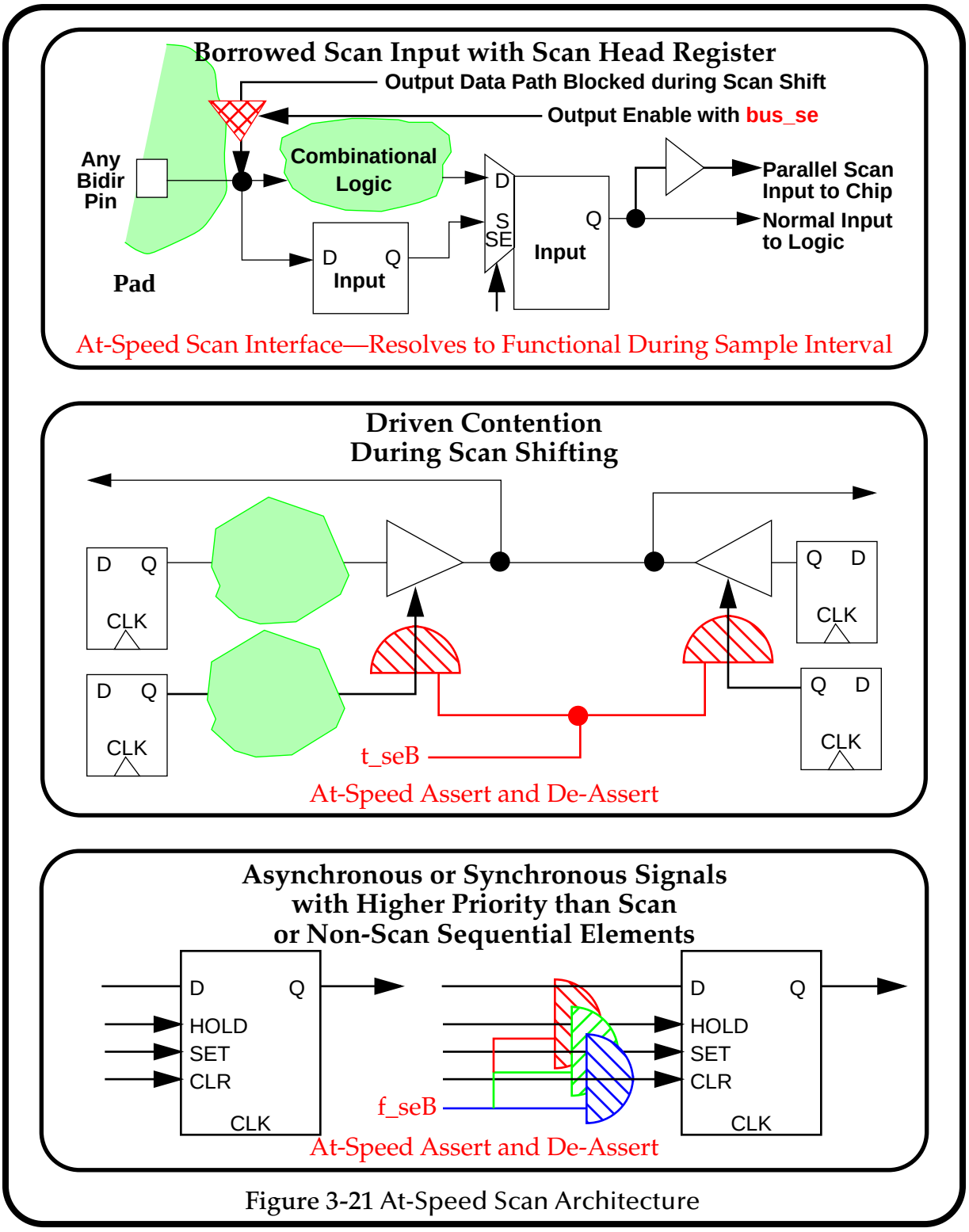


Figure 3-21 At-Speed Scan Architecture

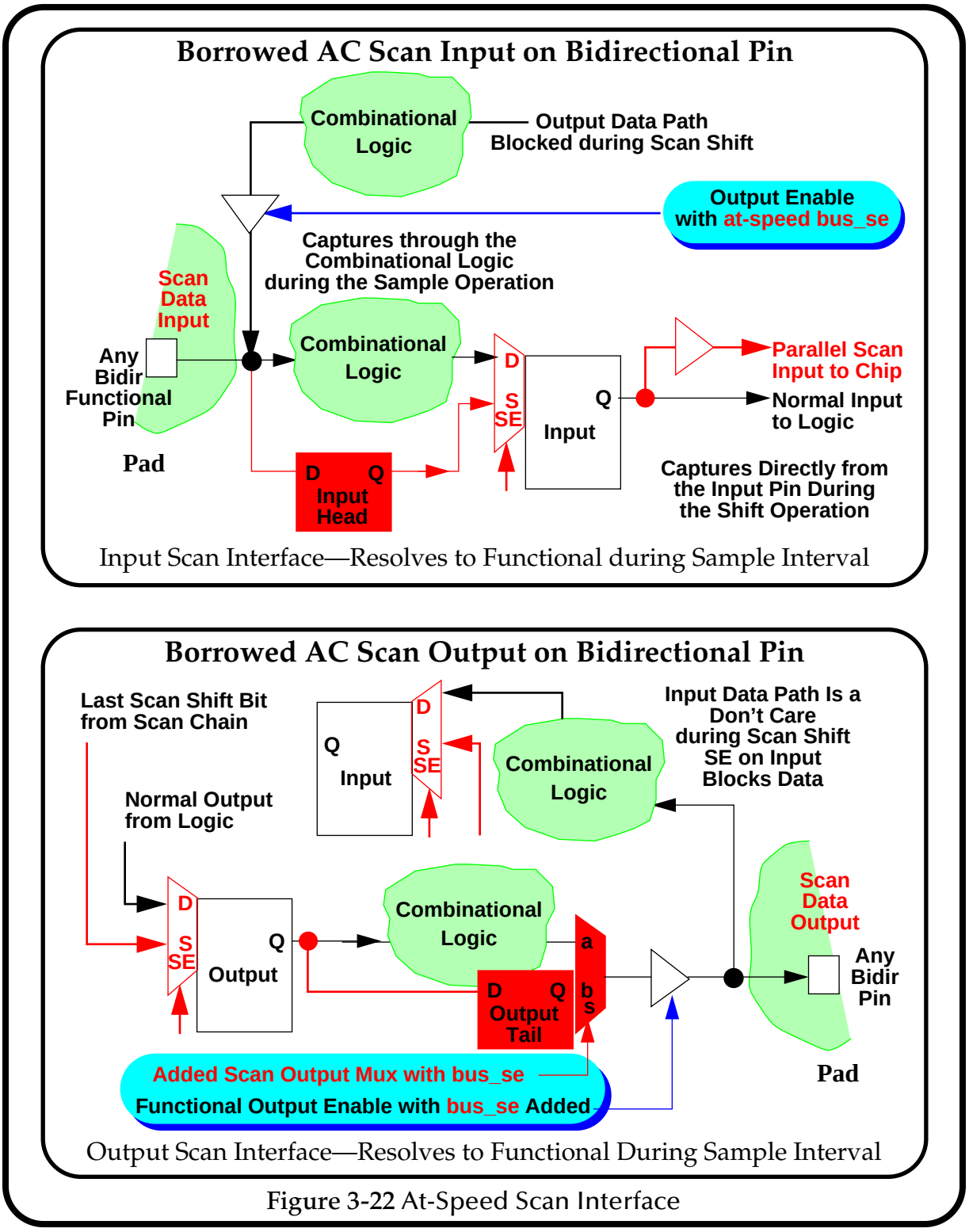


Figure 3-22 At-Speed Scan Interface

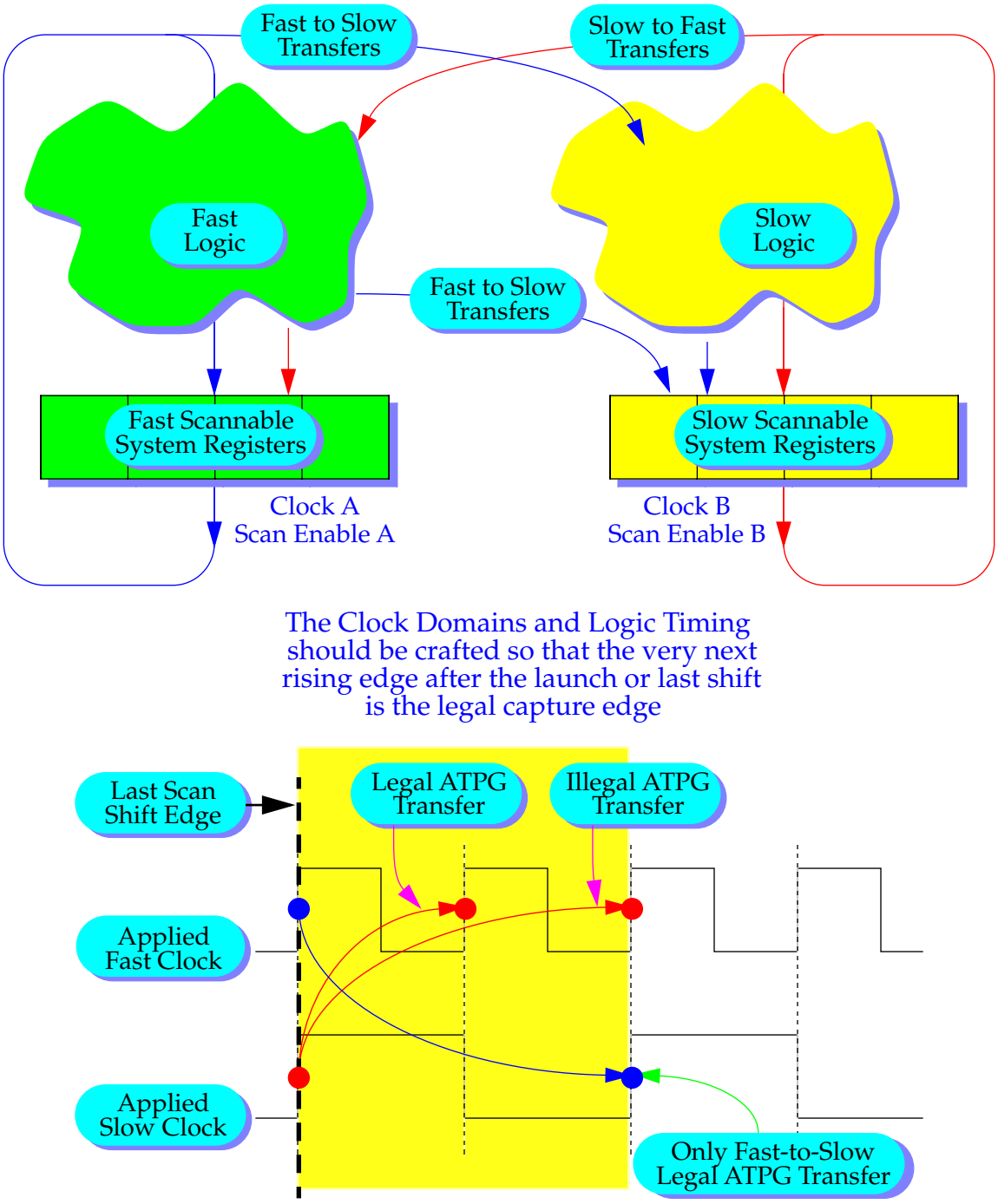


Figure 3-23 Multiple Scan and Timing Domains

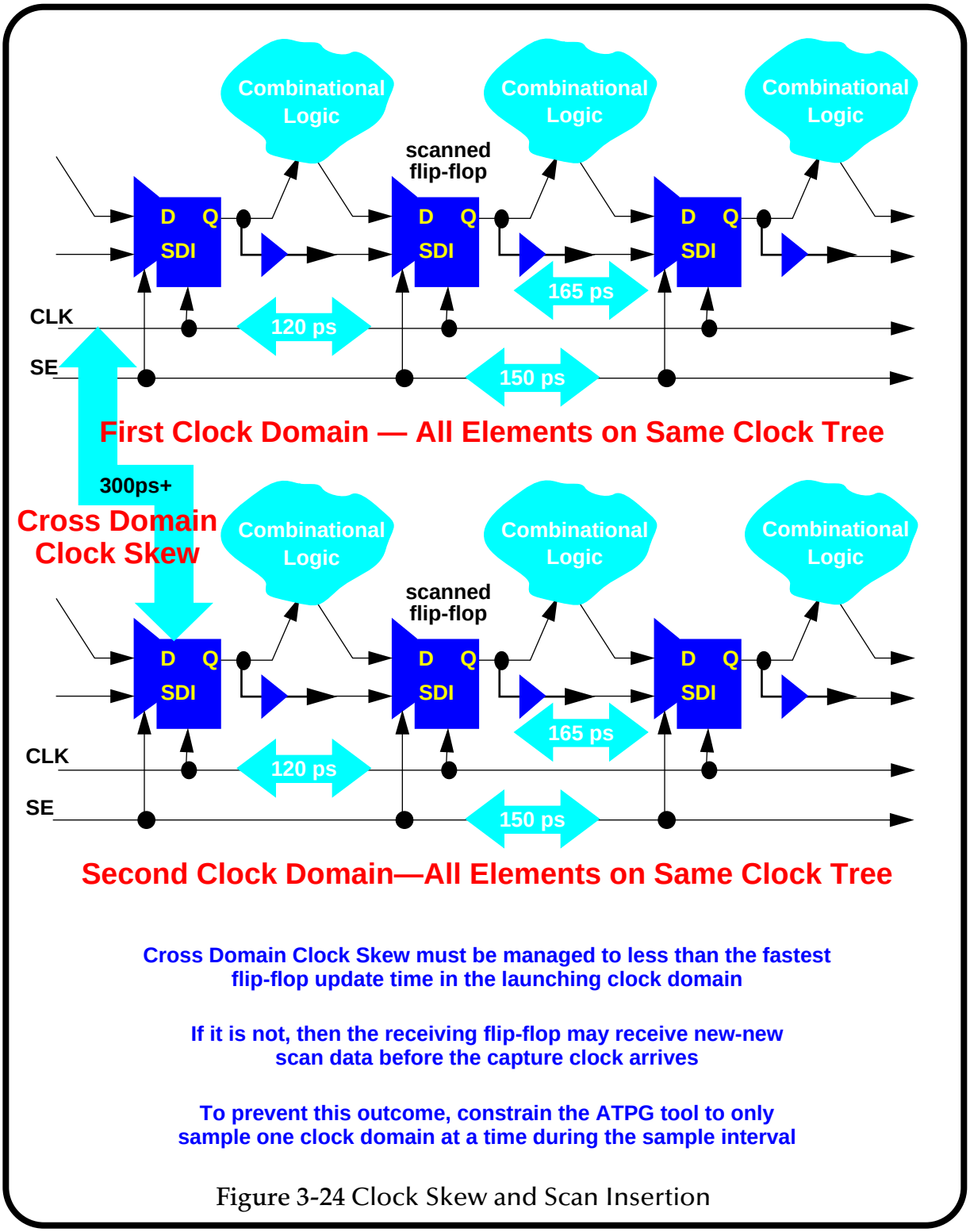


Figure 3-24 Clock Skew and Scan Insertion

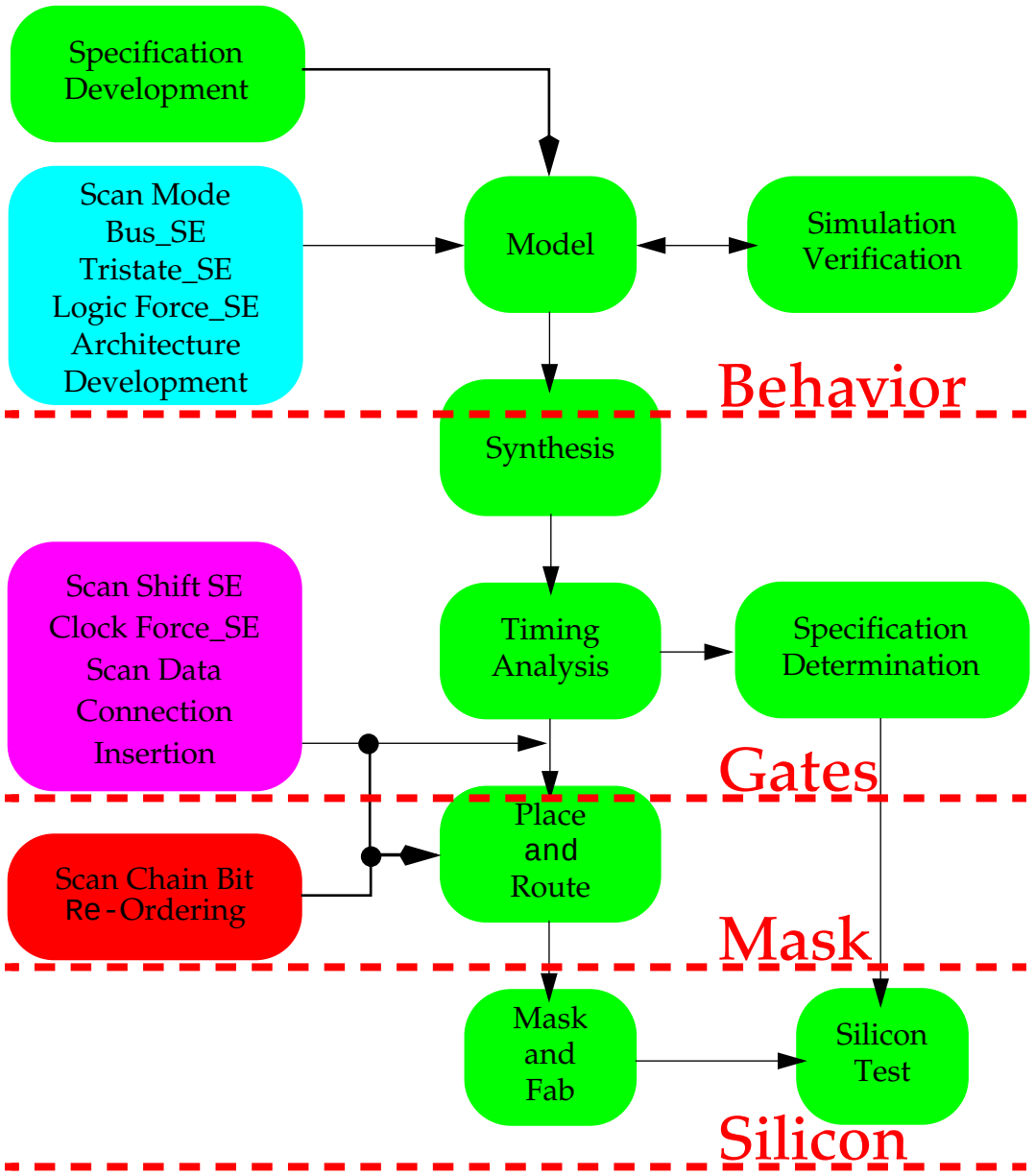
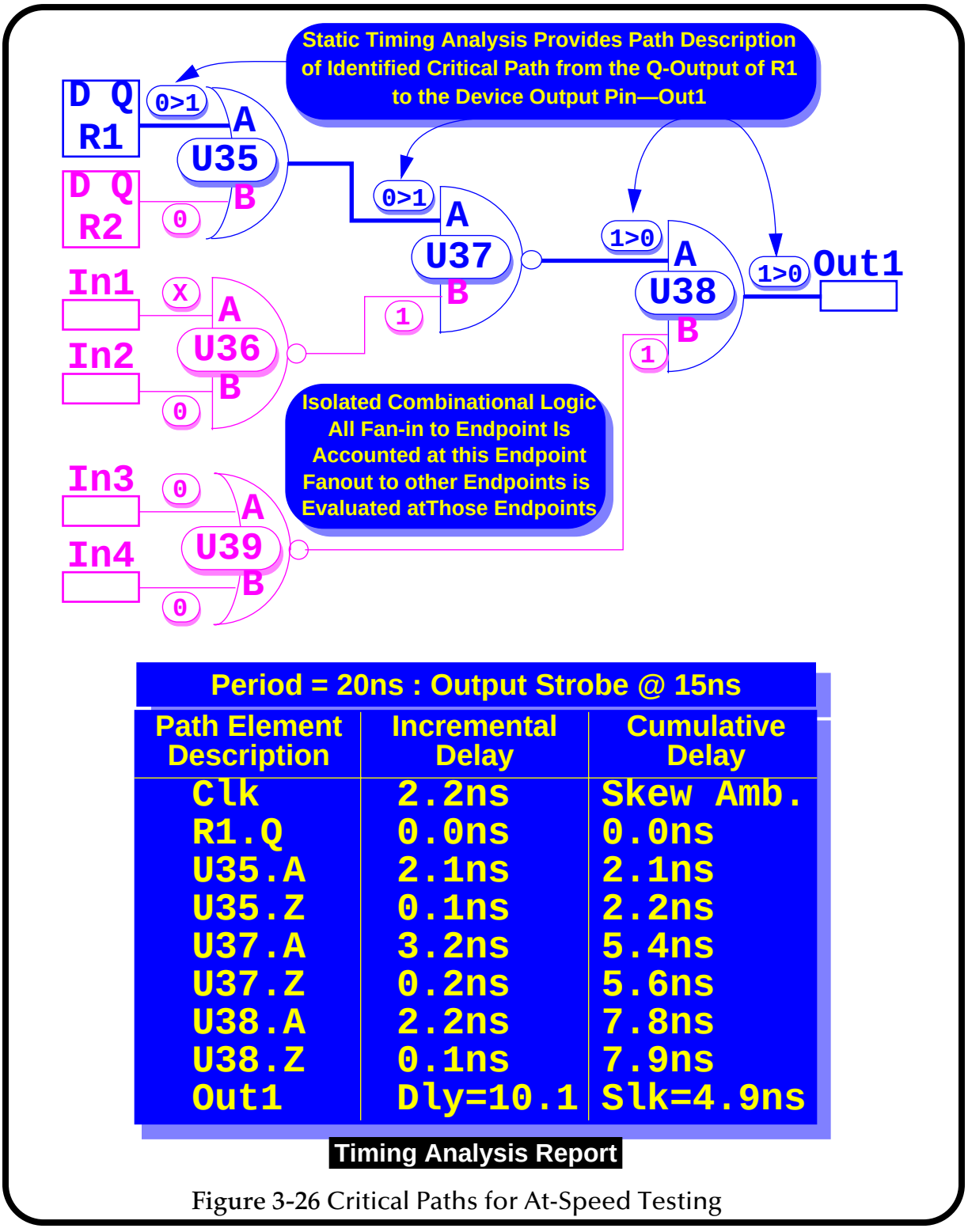


Figure 3-25 Scan Insertion for At-Speed Scan



Period = 20ns : Output Strobe @ 15ns

Path Element Description	Incremental Delay	Cumulative Delay
Clk	2.2ns	Skew Amb.
R1.Q	0.0ns	0.0ns
U35.A	2.1ns	2.1ns
U35.Z	0.1ns	2.2ns
U37.A	3.2ns	5.4ns
U37.Z	0.2ns	5.6ns
U38.A	2.2ns	7.8ns
U38.Z	0.1ns	7.9ns
Out1	Dly=10.1	Slk=4.9ns

Timing Analysis Report

Figure 3-26 Critical Paths for At-Speed Testing

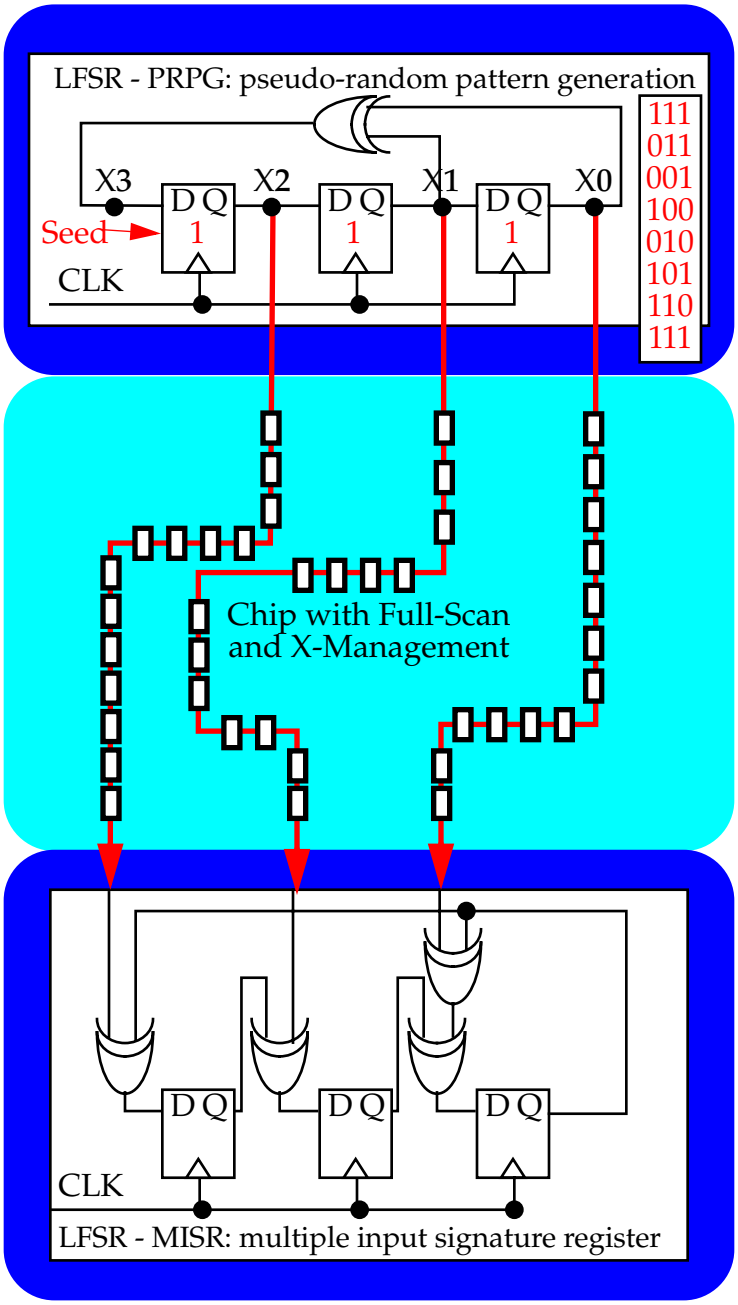


Figure 3-27 Logic BIST

Scan Testing Methodology

Advantages

Direct Observability of Internal Nodes

Direct Controllability of Internal Nodes

Enables Combinational ATPG

More Efficient Vectors

Higher Potential Fault Coverage

Deterministic Quality Metric

Efficient Diagnostic Capability

AC and DC Compliance

Concerns

Safe Shifting

Safe Sampling

Power Consumption

Clock Skew

Design Rule Impact on Budgets

Figure 3-28 Scan Test Fundamentals Summary