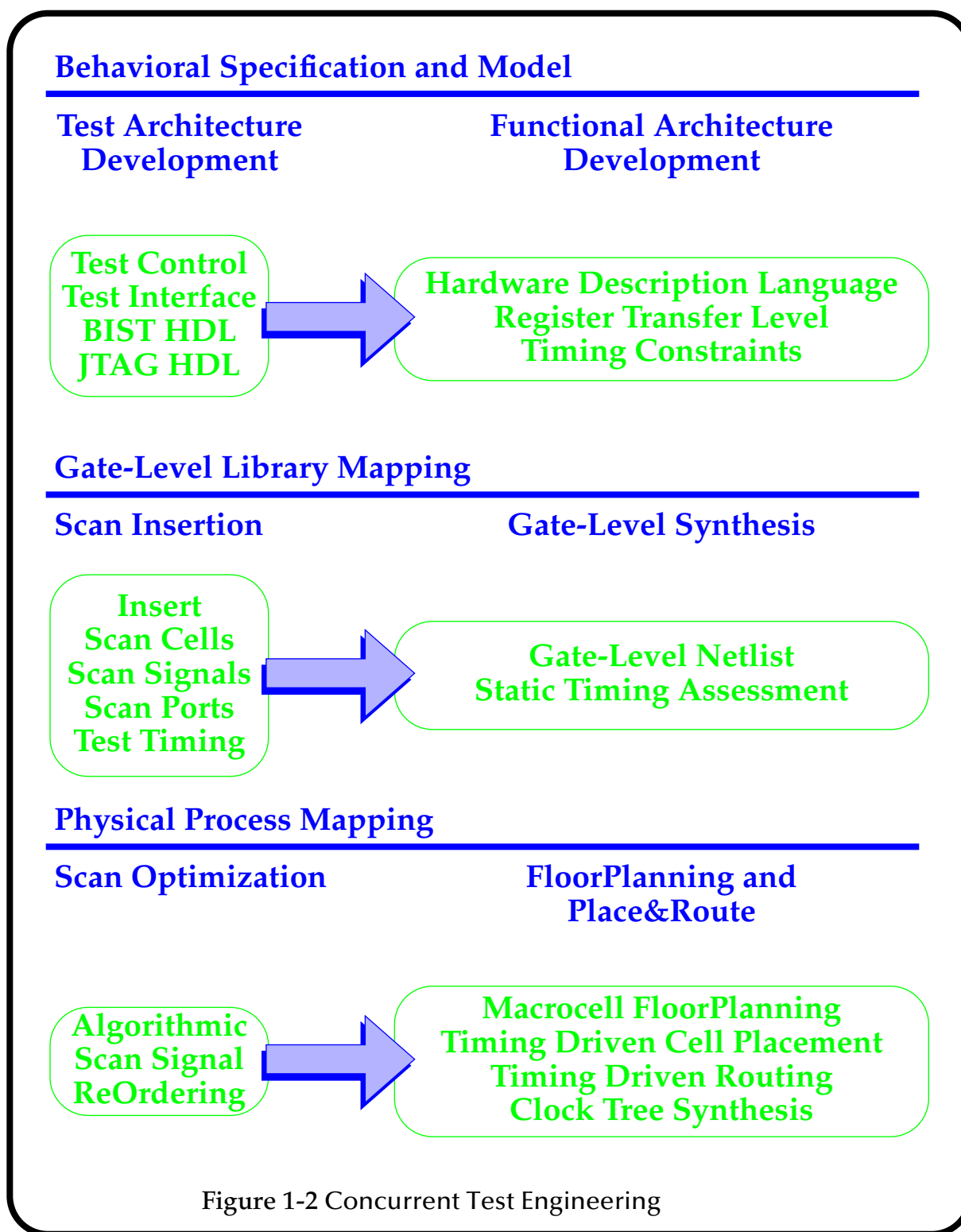**The goal over time is to reduce the cost of manufacturing the product by reducing the per-part recurring costs:**

- reduction of silicon cost by increasing volume and yield, and by die size reduction (process shrinks or more efficient layout)

- reduction of packaging cost by increasing volume, shifting to lower cost packages if possible (e.g., from ceramic to plastic), or reduction in package pin count

- reduction in cost of test by:
  - reducing the vector data size
  - reducing the tester sequencing complexity
  - reducing the cost of the tester
  - reducing test time
  - simplifying the test program

Figure 1-1 Cost of Product

Behavioral Specification and Model

Test Architecture   **Functional Architecture**
Development   **Development**

Test Control
Test Interface   →   **Hardware Description Language**
BIST HDL   **Register Transfer Level**
JTAG HDL   **Timing Constraints**

Gate-Level Library Mapping

Scan Insertion   **Gate-Level Synthesis**

Insert
Scan Cells
Scan Signals   →   **Gate-Level Netlist**
Scan Ports   **Static Timing Assessment**
Test Timing

Physical Process Mapping

Scan Optimization   **FloorPlanning and**
                                   Place&Route

Algorithmic   **Macrocell FloorPlanning**
Scan Signal   →   **Timing Driven Cell Placement**
ReOrdering   **Timing Driven Routing**
                          Clock Tree Synthesis

Figure 1-2 Concurrent Test Engineering

WHY TEST?

Reasons

Measurement of Defects & Quality Level

Incoming Inspection Contractual

Perceived Product Quality by Customer

Reliability Requirement Contractual

Pro & Con Perceptions of DFT

Eases Generation of Vectors

Adds Complexity to Design Methodology

Eases Diagnosis & Debugging

Impacts Design Power & Package Pins

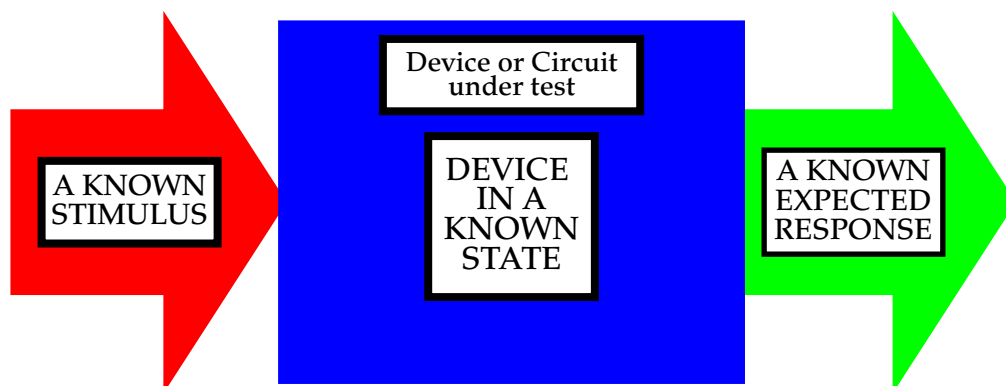Provides a Deterministic Quality Metric

Impacts Design Speed or Performance

Reduces the Cost of Test

Adds to Silicon Area
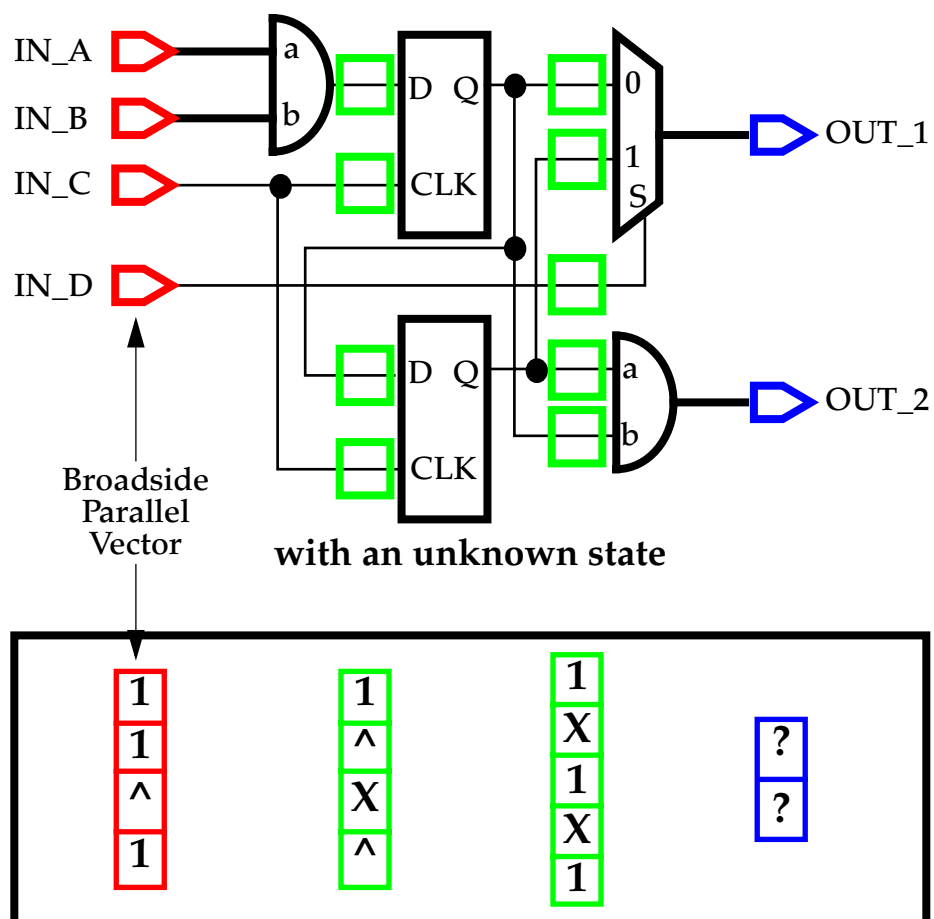
Figure 1-3 Why Test?

DEFINITION of TESTING

| A KNOWN STIMULUS | Device or Circuit under test / DEVICE IN A KNOWN STATE | A KNOWN EXPECTED RESPONSE |

EXAMPLE

IN_A

IN_B

IN_C

IN_D

a
b

D   Q

CLK

0
1
S

OUT_1

D   Q

CLK

a
b

OUT_2

Broadside Parallel Vector

with an unknown state

1	1	1	?
1	^	X	?
^	X	1	
1	^	X	
		1	

Figure 1-4 Definition of Testing

physical defects

opens
shorts
metal bridges
process errors

transistor faults

S 2 D	G2 D
S 2 G	G2 SB
S 2 SB	D2 SB

gate faults

a@ 0	a@ 1
b@ 0	b@ 1
c@ 0	c@ 1

observed truth table

A	B	C	failures
0	0	1	0
0	1	1	0
1	1	0	1
1	0	1	0

Transistor and Gate Representation of Defects, Faults, and Failures

Figure 1-5 Measurement Criteria

defects

open/short
bridge
mask
process

transistor faults

s 2 d	g 2 d
s 2 g	g 2 sb
s 2 sb	d 2 sb

stuck faults

a@ 0	a@ 1
b@ 0	b@ 1
c@ 0	c@ 1

6 gate faults

**transition
delay faults**

a1- 0	a0- 1
b1- 0	b0- 1
c1- 0	c0- 1

6 transitions

**Truth Table
with fail modes**

nand ab		a	b	c
ab c	0	1	1	0
00 1	1	1	1	0
01 1	1	0	1	0
10 1	1	1	0	0
11 0	1	0	0	0

**path
delay faults**

A2SR	A2SF
A2CR	A2CF
B2SR	B2SF
B2CR	B2CF

path

R=Slow-to-Rise
F=Slow-to-Fall

1 BIT ADDER with CARRY

Figure 1-6 Fault Modeling

Functional

$$3 + 5 = 8$$

Structural

1 BIT ADDER with CARRY

faultlist

a@ 0	a@ 1
b@ 0	b@ 1
e@ 0	e@ 1
f@ 0	f@ 1
r@ 0	r@ 1
t@ 0	t@ 1
s@ 0	s@ 1
c@ 0	c@ 1

16 faults
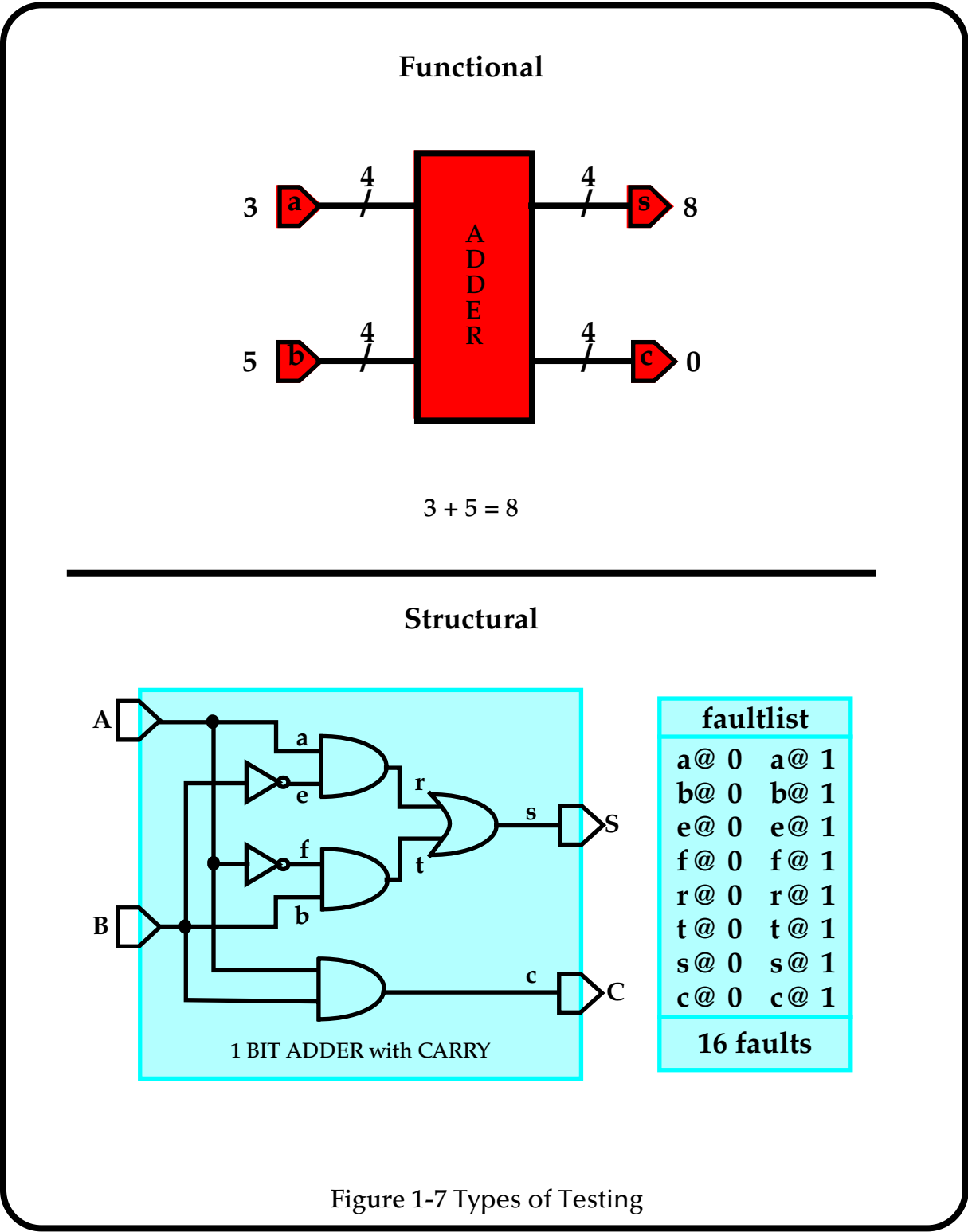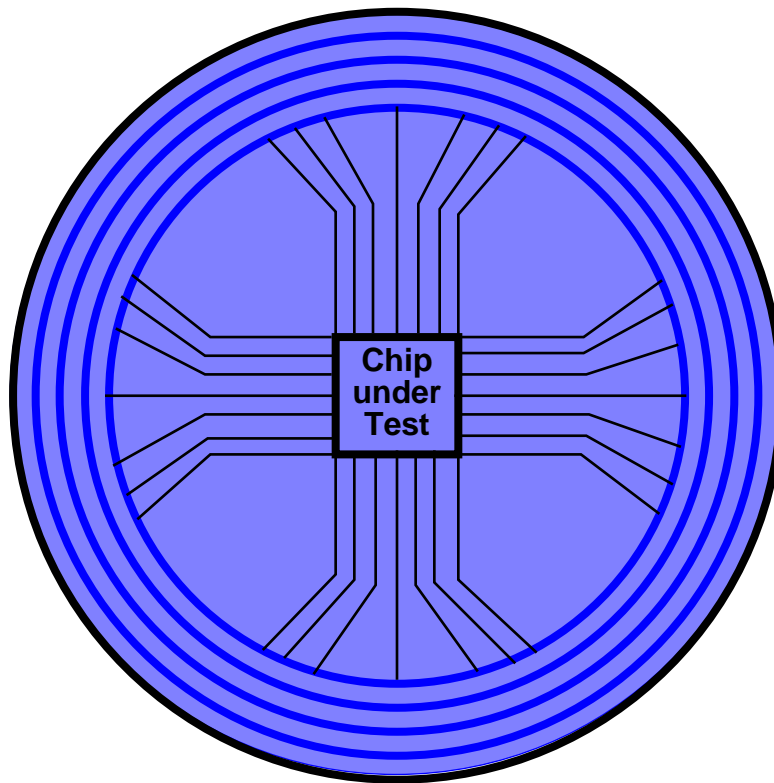
Figure 1-7 Types of Testing

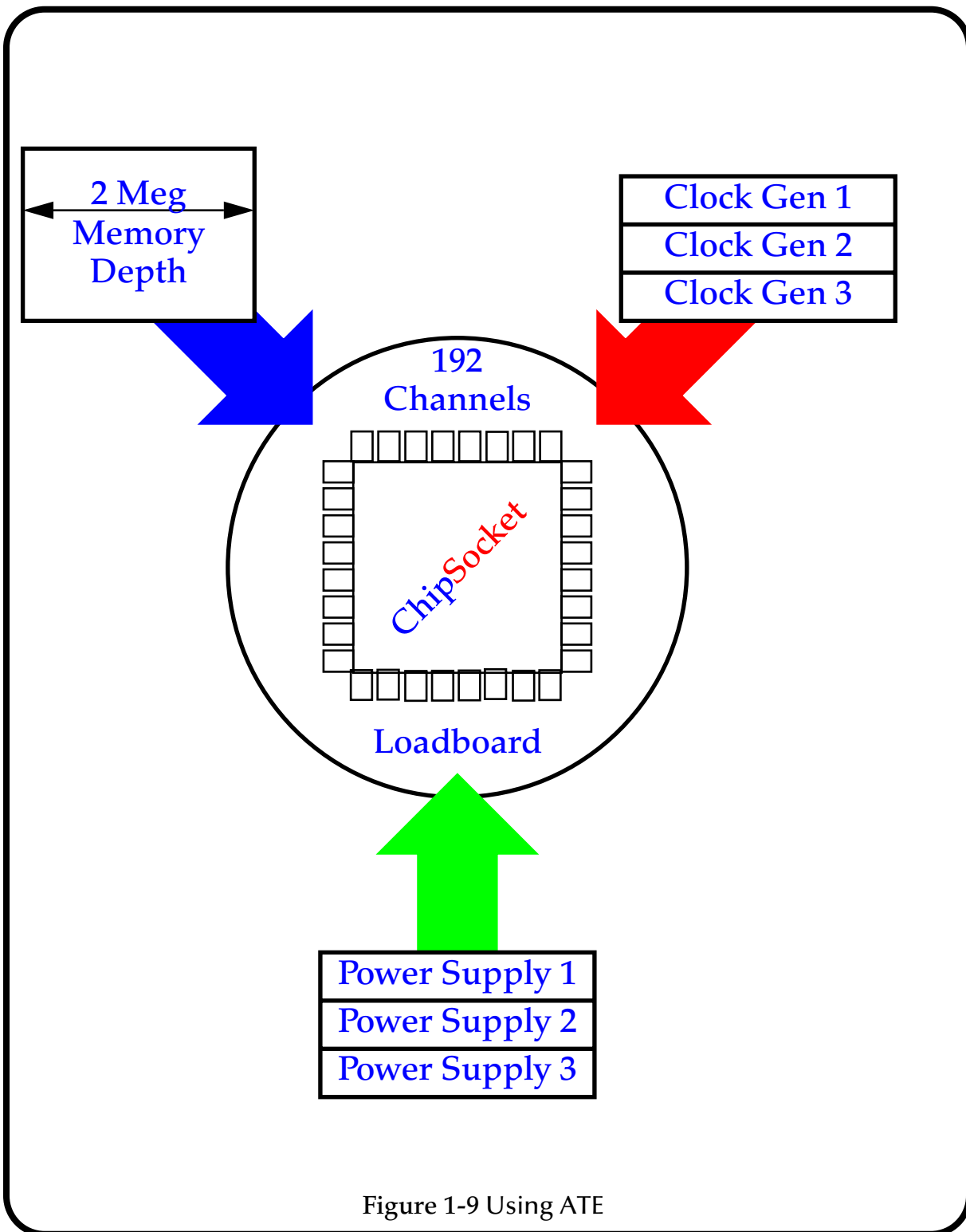The chip will be accessed by the tester at its pins only

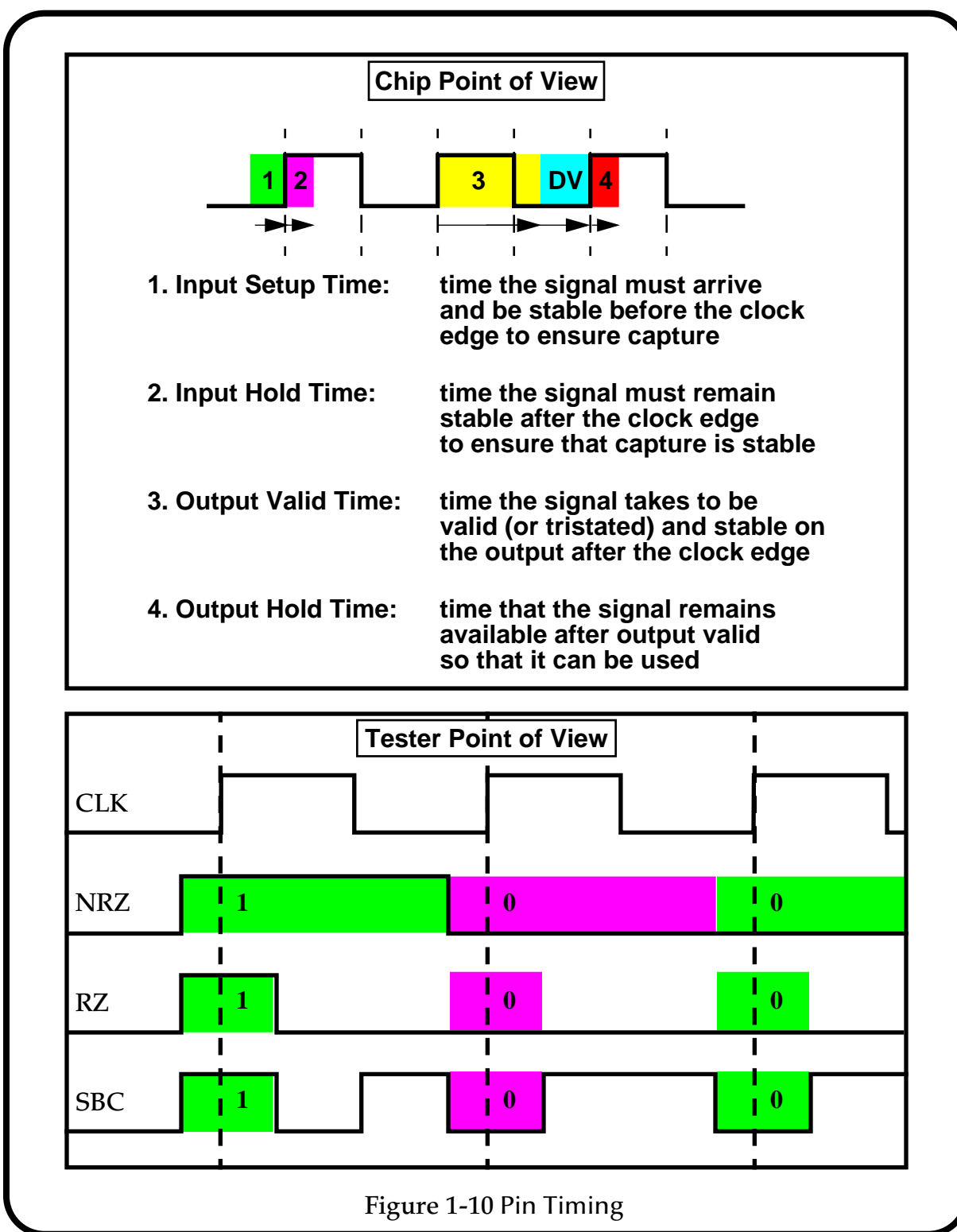A custom (load) board will be made for this purpose

Each pin has a limited number of bits available (e.g., 2 MB)

The test program (set of vectors and tester control) will be
applied at tester speed (may be less than actual chip speed)

The primary goal of manufacturing test is structural verification

Figure 1-8 Manufacturing Test Load Board

2 Meg Memory Depth

Clock Gen 1
Clock Gen 2
Clock Gen 3

192 Channels

ChipSocket

Loadboard

Power Supply 1
Power Supply 2
Power Supply 3

Figure 1-9 Using ATE

Chip Point of View

1. Input Setup Time: time the signal must arrive
                            and be stable before the clock
                            edge to ensure capture

2. Input Hold Time: time the signal must remain
                            stable after the clock edge
                            to ensure that capture is stable

3. Output Valid Time: time the signal takes to be
                            valid (or tristated) and stable on
                            the output after the clock edge

4. Output Hold Time: time that the signal remains
                            available after output valid
                            so that it can be used

Tester Point of View

Figure 1-10 Pin Timing

DC Pin Parametrics

Test Logic Verification

DC Logic Stuck-At

DC Logic Retention

AC Logic Delay

AC Frequency Assessment

AC Pin Specification

Memory Testing

Memory Retention

Idd and Iddq

Specialty Vectors

Analog Functions

Test Escapes

The Venn circles are examples of DC fault coverages of some of the vector classifications in the test program

Some of the fault coverages overlap

Vector reduction can be accomplished by removing overlap or by combining vector sets

Scan Path Delay

Scan Sequential
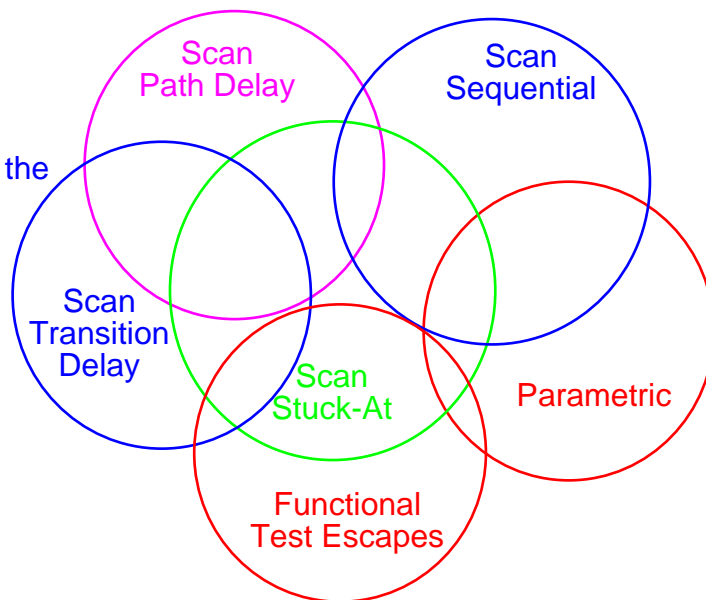
Scan Transition Delay

Scan Stuck-At

Parametric

Functional Test Escapes

Figure 1-11 Test Program Components