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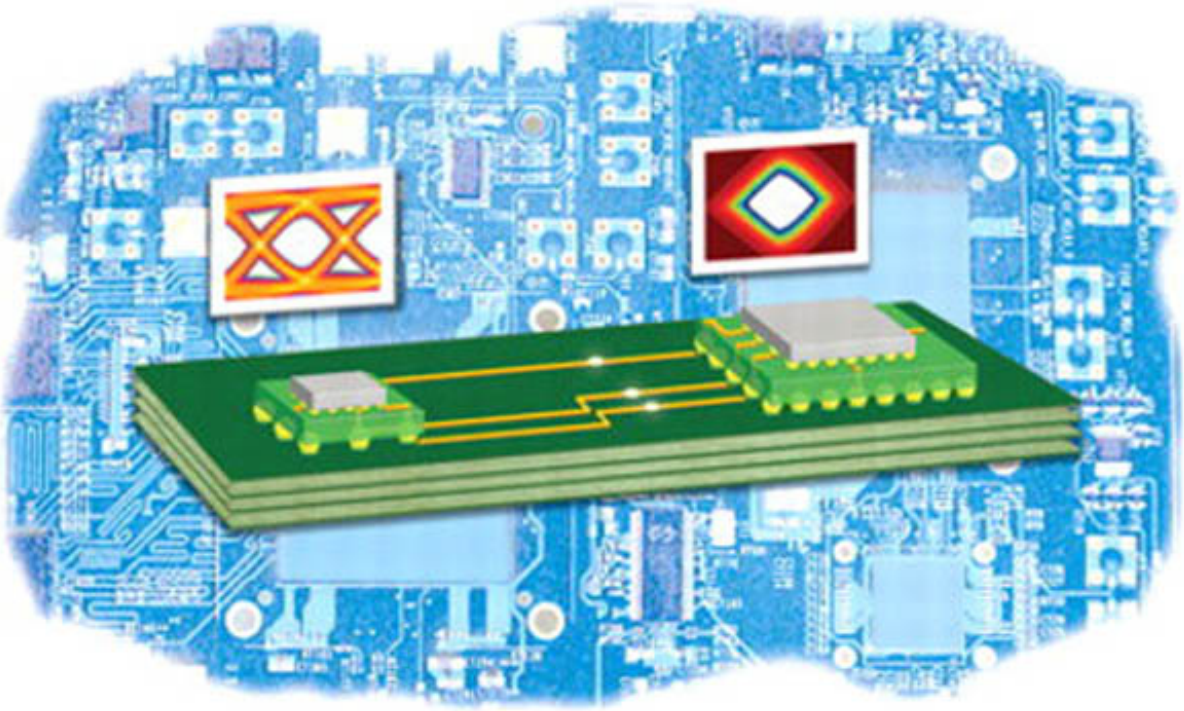
High-Speed Signaling:
Jitter Modeling, Analysis, and Budgeting



Kyung Suk (Dan) Oh and Xingchao (Chuck) Yuan

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HIGH-SPEED SIGNALING

Jitter Modeling, Analysis, and Budgeting

KYUNG SUK (DAN) OH
XINGCHAO (CHUCK) YUAN

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To my wife MyungSook, and our children, Terry and Christopher.
—Dan Oh

To my wife Jackie, my daughter Caterina, and my son Michael.
—Chuck Yuan

Contents

Preface

The majority of the books on signal integrity focus on techniques to validate and design physical passive channels, such as the package, printed circuit board, and power delivery network. Unfortunately, we cannot mitigate all signal integrity issues with package or board-level design improvements. Relying only on physical design improvements can lead to suboptimal or unrealistic system-level solutions. We must consider signal integrity issues at the early design stage of a modern high-speed I/O interface; engineers from various fields (such as architecture, circuit, system engineering, and signal integrity) must work together to find the best system-level solution for a target application.

This book serves as a bridge for engineers coming from different fields, because it is written from the perspective of I/O (input/output) link design. It starts with the basics of signaling components, which serves as a good starting point for circuit and architectural engineers who want to delve further into signal integrity issues. It also introduces the concept of I/O design, for the benefit of signal integrity and systems engineers.

Traditionally, I/O interface designs had clear boundaries for the roles for circuit, signal integrity, and systems engineers. Circuit designers designed a transceiver to meet the target performance requirements, using either a simplified channel model, or more complex channel models provided by the signal integrity engineers. Signal integrity or systems engineers designed the board and package to minimize signal-integrity issues, using either a simple behavior driver model, or a more accurate full-circuit model provided by the circuit designers. Although this approach is still widely used, it is no longer sufficient for today's high-performance systems. For instance, in high-speed I/O systems, noise and jitter (due to devices and boards) are no longer independent and separable: Engineers must co-optimize them in the circuit and board designs, sometimes even at the architectural level. To model this complex interaction of noise and jitter, modern high-speed interface designs need a new simulation methodology: one that predicts the accurate link-level performance (including the interaction of noise or jitter between the transmitter, receiver, and passive channel [such as packages and boards]). Traditional SPICE-based simulation approaches can no longer predict the performance of such a complex interaction. Some novel simulation methods have recently appeared in technical journals, and at conferences, but no comprehensive book has been written in this area. This book is perhaps the first book to systematically cover this new simulation methodology.

One of the lessons learned from the advances in power integrity engineering is that an ideal, stable power-delivery network design is no longer possible for modern power-hungry multi-core processors. Circuit designers have learned to design with significant power noise. Any

residual jitter or performance degradation due to power noise is budgeted for in the system margin. For example, in a high-speed I/O interface, the jitter induced by power supply noise is one of the dominant device-timing error terms. Consequently, power supply noise can no longer be budgeted for under the transistor voltage margin headroom. Additionally, this supply noise-induced jitter has broad frequency content, causing it to interact with the other parts of the channel, further complicating modeling issues. This book covers the basics of power supply–induced jitter, and describes characterization and simulation techniques.

Passive channel analysis and modeling has been, and still is, the main task for signal integrity engineers. Decades spent in the study of transmission-line modeling and macro modeling have given us fast channel simulations, but research is still in progress. Numerical inaccuracies or instability issues in transmission-line simulation or macro modeling methods are still some of the hottest topics at signal-integrity conferences. Until now, there has been no single numerical algorithm that provides a stable and accurate broadband model for general interconnect structures. Signal integrity engineers must understand the limitations of existing modeling methods, and apply them carefully. This book reviews the crucial limitations of some popular numerical models, and presents practical tips that you can use to avoid them.

This book is written for practicing engineers and managers working on high-speed system designs, as well as for professionals and graduate students doing research in this field. We have attempted to address all the latest issues and technologies with sufficient background and illustrations. Most of the information contained here has been verified, and has been widely used in real applications. Despite the fact that we have devoted significant effort toward making this book readable for entry-level engineers and graduate-level students, some of the advanced topics require some basic background on the part of the reader. As we cover different subjects from different engineering fields, the background requirements for individual chapters vary slightly. The minimum requirement is a basic knowledge of circuit theory. In addition, depending on the chapter, a basic knowledge of electromagnetics and/or statistics is required.

Acknowledgments

As illustrated by the long list of contributing coauthors, this book is the product of more than a decade of high-speed signal-integrity design experience on the part of many engineers at Rambus Inc. All the former, and current, Rambus SI engineers have contributed directly (or indirectly) to this book through their publications at Rambus. In addition to those listed as coauthors, these contributors include Dr. Wendem Beyene, Mr. Newton Cheng, Mr. Ben Chia, Ms. June Feng, Dr. Ching-Chao Huang, Dr. Cathy Huang, Dr. Woopoung Kim, Mr. Qi Lin, Mr. Frank Lambrecht, Dr. H.J. Liaw, Dr. Chris Madden, Dr. Xioning Qi, Mr. Ali Sarfaraz, and Ms. Ling Yang. As you can see from the contents of this book, the techniques discussed here go beyond the work of SI engineers. Specifically, the signal-integrity engineers at Rambus work closely with cross-functional teams that include architecture, circuit design, and system engineering. Many of these Rambus engineers have indirectly contributed to this book, in various ways, by working with us. We want to thank them all for their contributions. In particular, we want to distinguish a few individuals who have made direct contributions. The data coding (to reduce simultaneous switching noise) is largely the result of work done by Mr. Fred Ware, Dr. John Wilson, and Dr. Aliazam Abbasfar.

Special thanks also go to our former and current managers at Rambus. Without their support, this book would not have been possible. Particularly, we want to thank Mr. David Nguyen and Dr. Ely Tsern, whose encouragement made our work enjoyable. We also want to thank Mr. Kevin Donnelly, who provided some of the earliest encouragement when this book was just an idea. We also want to express our deep gratitude to Ms. Sharon Holt and to Mr. John Kent, both for their generous support, and for providing us with editorial resources.

Much of the transmission-line theory, and the recursive convolution method we describe, are based on the pioneering work done by Dr. Dmitri Kuzetzov and Prof. Jose Schutt-Aine. We want to thank them for their outstanding work and friendly discussions. The discussion on causality was inspired by discussions with Dr. Subramanian Lalgudi (Ansys). The editors also want to express our respect for the pioneering work of Prof. Mark Horowitz and his students. The on-chip measurement techniques and statistical simulation methodology described in this book were co-developed by Stanford University and Rambus, under Prof. Horowitz's guidance.

The editors also want to express our sincere gratitude to our reviewers: Dr. Dale Becker (IBM), Prof. Paul Franzon (NC), and Prof. Jose Schutt-Aine (UIUC) for their time and encouragement. These individuals are among the pioneers in the signal-integrity field, and their work laid the foundation for many of the topics covered in this book.

Our appreciation also goes to the Prentice Hall editors and staff, including Bernard Goodwin, Betsy Harris, Paula Lowell, Debbie Williams, and Michelle Housley, for their editorial

support and encouragement. Mr. Greg Morris is also gratefully acknowledged, for his grammatical editing and document formatting. The editors also want to thank Ms. Yi Jiang for providing the cover picture.

Finally, we are deeply indebted for the support that we received from our families: Dan's wife Myung (and sons Christopher and Terry), and Chuck's wife Jackie (and daughter Caterina and son Michael); who supported us through their endless love. This book is a result of more than three years of effort. In particular, we want to thank our kids, for their encouragement, when they kept asking us "Dad, have you finished your book yet?" Without our family's love and support, which allowed us to work countless weekends and nights, this book would not be possible.

DAN OH AND CHUCK YUAN

About the Authors

Kyung Suk (Dan) Oh received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana-Champaign, in 1990, 1992, and 1995, respectively. His doctoral research was in the area of computational electromagnetics applied to transmission line modeling and simulation. He is a Senior Principal Engineer at Rambus Inc. He leads signal integrity analysis for various products including serial, parallel, and memory interfaces. He is also responsible for developing advanced signal and power integrity analysis tools. His current interests include advance signal and power integrity modeling and simulation techniques, optimization of channel designs for various standard or proprietary I/O links, and application of signaling techniques to high-speed digital links.

Dr. Oh has published more than 80 papers and holds 7 issued U.S. patents and 10 pending patent applications in areas of high-speed link design. He received two Best Paper Awards in DesignCon and 2008 Best Paper Award in the IEEE Advanced Packaging journal. Dr. Oh serves on the technical program committee of IEEE EPEPS, and is a former member of the IEC DesignCon Technical Program Committee.

Xingchao (Chuck) Yuan received his B.S. degree in Electronic Engineering from Nanjing Institute of Technology (now Southeast University), Nanjing, China, in 1982. He received both his M.S. and Ph.D. degrees in Electrical Engineering from Syracuse University, Syracuse, New York, in 1983 and 1987, respectively. After receiving his Ph.D., Dr. Yuan was at the Thayer School of Engineering at Dartmouth College; first as a Postdoctoral fellow, and later as a Research Professor from 1987 to 1990.

From 1990 to 1995, Dr. Yuan was employed by Ansoft Corp., where he led the development of Ansoft's flagship product *HFSS*™ (High Frequency Structure Simulator). His work led to three different product releases, which included features such as modeling conductor and dielectric loss, radiation and periodic boundary conditions for modeling antennas, and electromagnetic scattering/interference problems. He pioneered a fast frequency sweep method that combined a finite element method and an asymptotic waveform evaluation method. This led to a dramatic speed improvement in the speed of 3D full-wave modeling. From 1995 to 1998, Dr. Yuan was with Cadence Corp. where he led the research and development of the signal integrity and EMI tools. His work focused on modeling SSO noise and induced electromagnetic interference, which led to some of the earliest research in power plane modeling.

Since 1998, Dr. Yuan has been with Rambus Inc, Sunnyvale, California, as a director of signal integrity engineering. Dr Yuan is responsible for designing, modeling, and implementing Rambus multi-gigahertz signaling technologies using conventional interconnect technologies.

His technical and managerial leadership at Rambus has led to an industry-recognized signal and power integrity team of experts. Rambus' SI/PI papers are closely followed by the rest of the industry, and represent the latest developments in high-performance signal and power integrity modeling and design. Dr. Yuan's team was among the first to apply BER and statistical methodology to memory interface designs, and to explore the relationship between the supply noise spectrum and the jitter spectrum. His team's work led to the successful development of Rambus' XDR memory architecture, which was adopted by PlayStation® 3, DLP projectors, and DTVs. Since 2009, Dr. Yuan has served as an engineering director in charge of a silicon team with dozens of engineers (in both the U.S. and India) who are responsible for designing next-generation Rambus graphics and main memory interfaces. In 2010, the team taped out a multi-modal PHY that explores the limits of single-ended signaling beyond 12.8Gbps, a power efficient differential interface at 20Gbps, and backward compatibility with existing memory interfaces (including GDDR5 and DDR3).

Dr. Yuan has authored more than 100 papers in technical journals and conferences and holds 8 issued U.S. patents. He is a senior member of IEEE, and served on the technical program committee of IEEE EPEPS from 2008 to 2009.

Jihong Ren received her Ph.D in Computer Science from the University of British Columbia in 2006. Since January 2006, she has been with Rambus working on high-speed link analysis, adaptive equalization algorithms, advanced signaling schemes, and circuit analysis. She was the recipient of the Best Paper Award from the IEEE Transactions on Advanced Packaging Journal for 2008.

Hai Lan is a Principal Engineer at Rambus Inc., where he has been focusing on on-chip power integrity and jitter analysis in high-speed and/or low-power I/O interfaces, specializing in advanced modeling, simulation, and on-chip characterization. He received his Ph.D. degree in Electrical Engineering from Stanford University in 2006. His doctoral research focused on substrate coupling noise in mixed-signal ICs and SoC. He received his M.S. in Electrical and Computer Engineering from Oregon State University in 2001, where he developed closed-form expressions for frequency-dependent on-chip interconnect parameters. He received his B.S. in Electronic Engineering from Tsinghua University in 1999. His professional interests include power integrity and signal integrity, mixed-signal integrated circuits design, high-speed interconnects modeling, and advanced silicon effects such as substrate noise coupling.

Ralf Schmitt received his Ph.D. in Electrical Engineering from the Technical University of Berlin, Germany. Since 2002, he has been with Rambus as an engineering manager responsible for power integrity at the chip, package, and system level. His professional interests include on-chip signal integrity, power integrity, timing analysis, clock distribution, and high-speed digital circuit design.

Sam Chang is currently an engineer in the Signal Integrity Division at Rambus. His current work involves the modeling and development of solutions for high-speed digital links. Dr. Chang holds

a Ph.D. in Electrical Engineering (2005) from University of California, Riverside. He has published more than 20 papers in areas of high-speed link design and digital communications. He received the 2008 Best Paper Award in the IEEE Advanced Packaging journal.

Joong-Ho Kim received his Ph.D. degrees in electrical and computer engineering from Georgia Institute of Technology, Atlanta, Georgia, in 2002. During his graduate study, he worked at the Packaging Research Center (PRC), where he researched efficient electrical modeling techniques for analyzing packages/systems. As a result of his research, Dr. Kim developed transmission matrix and macro-modeling methods for analyzing large and complex power delivery networks.

In 2005, Dr. Kim joined Rambus. He is currently a Principal Engineer in the Technology Development Division. He is responsible for product/technology design and analysis in signal/power integrity (SI/PI) area for high-performance memory interface products (such as XDR, DDR2/3, GDDR3/4/5, Mobile XDR, and LPDDR1/2), and next generation mobile, computing, and graphic memory systems. Previously, he worked on SI/PI analysis for CMOS microprocessors and in-house tool developments at Intel Corporation. His current research interests are a systematic approach that considers both signal and power integrity simultaneously, characterization of high-speed interconnects, S-parameter–based simulations using VNA measurements or full-wave solvers, and macro modeling for circuit simulations.

Dr. Kim has published more than 40 papers in journals and conferences, one book (as a chapter author in the IEC conference publications), and has nine issued patents. He received the Best Paper Award at EPEP 2000, 1st Place Poster Award at NSF-PRC 2000, Best Paper Award at Intel DTTC 2004, and two Best Paper Awards at IEC DesignCon 2008.

Ravi Kollipara is a Senior Principal Engineer responsible for the signal integrity of high-speed serial links and parallel bus channels. His duties include design and characterization of channel passive components (such as packages and PCBs), measurement-based modeling of connectors, and development of system voltage and timing budgets. He has been with Rambus since 1998. Prior to joining Rambus, Dr. Kollipara worked at LSI Logic and taught as a visiting assistant professor. He received his B.E, M.Tech, and Ph.D. degrees from Andhra University, IIT Delhi, and Oregon State University, respectively.

Jared Zerbe graduated from Stanford University, Stanford, California, in 1987. From 1987 to 1992, he was with VLSI Technology and MIPS Computer Systems. In 1992, he joined Rambus, where he has since specialized in the design of high-speed I/O, PLL/DLL clock-recovery, and equalization and data-synchronization circuits. He has authored multiple papers and has been awarded patents in the areas of high-speed clocking and data transmission. Mr. Zerbe has taught courses at Berkeley and Stanford in link design. He is currently a Technical Director, and focuses on the development of future signaling technologies.

Hao Shi received his B.S. degree in microelectronics from Beijing University in 1984, M.S.-Physics degree in Physics from University of Missouri-Kansas City in 1993, M.S.-E.E. and

Ph.D.-E.E. degrees from Missouri University of Science and Technology (also known as University of Missouri-Rolla) in 1995 and 1997, respectively. Between 1984 and 1993, he was involved in material science research of high-Tc superconductors, specializing in measurements. From 1998 to 2002, he was with Hewlett-Packard and Agilent Technologies, holding engineer positions in the fields of EDA, analog, and microwave designs. From 2002 to 2008, he was with Rambus Inc. as a signal integrity engineer. He is currently with Apple, Inc. as a principal SI Engineer. His professional interests include modeling and simulation of interconnects in PCB and packaging, power delivery system decoupling, noise containment of switched-mode power supplies, connector modeling, and electromagnetic compatibility.

On various subjects concerning signal integrity, Dr. Shi has published 8 peer-reviewed journal papers (as the first author in 4), and 17 conference papers (as the first author in 8). He was one of the lead authors of the issued U.S. Patent No. 7476813 as well as the patent application No. 20100096725, both of which are related to packaging designs. He was the winner of the President's Memorial Award from the IEEE-EMC society in 1995, and he is currently a senior member of the IEEE.

Vladimir Stojanovic is the Emmanuel E. Landsman Associate Professor of Electrical Engineering and Computer Science at MIT. His research interests include design, modeling and optimization of integrated systems, from CMOS-based VLSI blocks and interfaces to system design with alternative devices (such as NEM relays and silicon-photonics). He is also interested in the design and implementation of energy-efficient electrical and optical networks, and in digital communication techniques for high-speed interfaces and high-speed mixed-signal IC design. He is a recipient of the 2009 NSF CAREER award.

Dr. Stojanovic received his Ph.D. in Electrical Engineering from Stanford University in 2005. He received his M.S. degree in Electrical Engineering from Stanford University in 2000, and the Dipl. Ing. degree from the University of Belgrade, Serbia, in 1998. He was with Rambus from 2001 through 2004. He was also a visiting scholar with the Advanced Computer Systems Engineering Laboratory, Department of Electrical and Computer Engineering, University of California, Davis, during 1997–1998.

Elad Alon received B.S., M.S., and Ph.D. degrees in Electrical Engineering from Stanford University in 2001, 2002, and 2006, respectively. In Jan. 2007, he joined the University of California at Berkeley as an Assistant Professor of Electrical Engineering and Computer Sciences, where he is now a co-director of the Berkeley Wireless Research Center (BWRC). He has held positions at Sun Labs, Intel, AMD, Rambus, Hewlett-Packard, and IBM Research, where he worked on digital, analog, and mixed-signal integrated circuits for computing, test and measurement, and high-speed communications. Dr. Alon received the IBM Faculty Award in 2008, the 2009 Hellman Family Faculty Fund Award, and the 2010 UC Berkeley Electrical Engineering Outstanding Teaching Award. His research focuses on energy-efficient integrated systems, including the circuit, device, communications, and optimization techniques used to design them.

CHAPTER 1

Introduction

Dan Oh and Chuck Yuan

Computing devices, such as computer servers, workstations, personal computers, game consoles, and smart phones, have become increasingly more powerful with each new generation of semiconductor process. Thanks to Moore's Law, which states that the number of transistors on a chip doubles every two years [1], there is not only more functionality available for a given device, but also an increase in performance. To keep up with the increase in performance, the data communication speed between the components of the computing device has also been increasing, rising from a few hundred Mb/s in the early 1990s to several Gb/s in 2008. It is projected that data communication rates will soon increase to tens of Gb/s. For instance, the next generation PCIe specification is considering 8Gb/s as a target data rate and is expected to be in production by 2012.

As data communication reaches multi-gigabit/sec rates, the task of ensuring good signal integrity, both on-chip and off-chip, becomes increasingly important. Understanding the high-frequency physical effects introduced by the wire or interconnect is as important as the silicon design itself. Moreover, device jitter (generated by on-chip circuitry) now becomes a signal-integrity (SI) problem, because system-level behavior (such as jitter amplification and cancelation) must be modeled. The time when signal integrity was considered, only after the silicon was built, has passed. The I/O interface designer, or system designer, must perform a thorough signal-integrity analysis to avoid producing non-reliable or overly constrained systems, or incurring costly recalls of products from the marketplace.

Signal-integrity design considerations must be considered upfront to ensure the robust operation of modern high-speed digital systems. New design methodologies must be introduced and employed to account for the physical effects that could be ignored at lower data rates. To minimize timing errors with the new target data rates and channel designs, clocking or timing circuitry designs must be optimized. Before building any hardware or system, worst-case design

parameters and interconnect electrical behavior must be evaluated and analyzed. A detailed and accurate understanding of the electrical behavior of interconnect, advanced signaling, and circuit techniques (such as equalization) can be used to overcome the non-ideal effects introduced by interconnects.

Accurate prediction of system behavior at multi-gigabit data rates is a challenging task that requires a signal-integrity engineer who possesses knowledge of, and experience in, several diverse engineering disciplines. Specifically, such an engineer must have knowledge of digital system engineering, high-speed I/O circuit design, electronic package and printed circuit board design, communications theory, microwave engineering, and computational electromagnetics. Because of these multi-disciplinary requirements, signal-integrity engineers come from many different technical backgrounds, such as circuit and printed circuit board design, RF/microwave engineering, and electromagnetic modeling. The signal-integrity engineer then gains the necessary knowledge and experience on the job. Few universities offer courses and training programs that specifically teach signal integrity, which contributes to the growing shortage of signal integrity engineers.

Because signal integrity is a relatively new, fast-evolving, and multi-disciplinary field, few good reference books exist on the subject. H.B. Bakoglu's book, published in 1990, is a good introduction to signal integrity [2]. Bakoglu's primary audience is the silicon circuit designer who wants to understand the impact of interconnects on high-speed data transmission. H. W. Johnson's book, published in 1993 [3], is a practical handbook for signal integrity engineers. W. Dally's work, published by Cambridge University Press in 1998 [4], offers comprehensive information on high-speed digital system design. It offers excellent information about designing high-speed signaling systems by considering the impact of circuit design, packaging and interconnect design, and power distribution network design. Recently, more books on signal integrity design and engineering have become available [5–19]. Those books cover a wide range of topics, including printed circuit board design, system timing analysis, substrate noise coupling, and power supply noise modeling.

Although the aforementioned books have been very useful to signal integrity engineers, most of them focus on one specific topic. Few take a systematic approach and discuss how to design a high-speed system from the architecture design phase to production, or how to ensure robust system operation under worst-case operating conditions. Finally, few offer information about how to achieve maximum system yield for high-volume manufacturing. Some of the material is now outdated, because the data rates have increased from a few megabits to several gigabits. As a result, signal-integrity engineers, who must confront the new challenges of multi-gigabit designs, lack adequate reference material. They must study topics that are common in communication theory, circuit theory, microwave engineering, and computational electromagnetic theory to understand and design a multi-gigahertz system.

This book offers a comprehensive discussion of high-speed signal integrity engineering. It is intended as an intermediate to advanced text to aid signal-integrity engineers in acquiring the necessary skills and knowledge needed to design and model multi-gigabit digital systems. It

assumes the reader has some basic understanding of various electrical engineering subjects, such as VLSI design, transmission-line theory, and microwave engineering. This book draws on 10 years of high-speed signal integrity design experience, from more than two dozen engineers at Rambus Inc. Rambus®-designed I/O interfaces have had a wide range of data rates, ranging from 800Mb/s in the early 1990s, to 16Gb/s in 2009. Most Rambus I/O interfaces have been proprietary, and SI engineers have worked closely with other circuit and architecture engineers to ensure reliable channel performance. SI engineers were involved in defining signaling definitions and circuit requirements, characterizing and simulating a prototype virtual channel, and accounting for mass production environments. This book shares more than a decade of collective experience in analyzing various I/O interfaces, such as on-board parallel busses, backplanes, consumer memory, and PC main memory.

What is unique about this book?

- This book takes a systematic approach and considers signal integrity from the architecture phase to high volume production.
- This book covers a broad range of topics, including the design, implementation, and verification of high-speed I/O interfaces.
- Passive-channel modeling, power-supply noise and jitter modeling, as well as system margin prediction, are considered in extraordinary depth.
- Both signal integrity (SI) and power integrity (PI) are considered in a holistic approach, designed to capture actual system behavior. The impact of power noise-to-signal quality (including both on-chip and off-chip noise) is also considered.
- Methodologies for balancing system voltage and timing budget are explained in detail to help ensure system robustness in high-volume manufacturing.
- Practical, yet stable, formulae to convert various network parameters are described for the first time, as network and transmission line theories are an important part of channel analysis. Broadband modeling of interconnects is quite challenging. Some fundamental issues with existing models and tools are described, along with potential improvements and tips to avoid inaccurate models.
- This book takes a systematic approach, and considers signal integrity from the architecture phase to high volume production.
- This book presents the most recent advances in SI and PI engineering. Specifically, equalization techniques to improve channel performance are explained at a high level. High-volume manufacturing modeling and link jitter/statistical simulation methodologies are covered for the first time. The relationship between jitter and clocking topology is explored in detail. On-chip measurement techniques for in-situ link performance testing are also presented.

1.1 Signal Integrity Analysis Trends

Signal-integrity engineering is a relatively new engineering discipline; its development is driven by the need to design high-speed digital systems. In the early 1990s, when digital systems were relatively slow in terms of operating data rates, signal integrity was often an afterthought. Engineers did not have to worry much about the parasitic effects of passive interconnect, which includes package and printed circuit board traces, via transitions, and connectors. The physical designs of the package and PCB were often simply "connecting dots" in layout tools. However, as the data rates of the high-speed systems increased, people encountered numerous system failures due to parasitic effects, such as crosstalk, reflections, and power-supply noise. As a result, signal integrity engineering has grown from relative obscurity into one of the most important engineering disciplines. This section reviews the history of signal-integrity engineering, discusses its evolution over the past decade, and explores its future directions.

1.1.1 Pre-1990: Era of "Black Magic"

During the early days of the computer, transistor device speed limited the I/O speed. As a result, the parasitic effect on the digital system was negligible. There was no need to be concerned about signal integrity, unless one was designing super computers. During this period, the noise problems related to crosstalk and supply noise were addressed on a case-by-case basis. The necessity of trying to debug system failures drew engineers, with various technical backgrounds and experience, to SI engineering. Typical engineering backgrounds included analog design, I/O circuit design, printed circuit board (PCB) and package design, microwave engineering, and electromagnetic modeling. In fact, SI tasks were considered a "side job," rather than as a primary job function.

During these early days, SI engineering was in its infancy. Several problems typified the period: First, the physics of noise in digital systems was poorly understood. Though parasitic effects at high frequency were well studied in related microwave engineering, little knowledge was transferred to digital design. Second, digital designers ignored the impact of parasitic effects during the design phase. The problem was addressed only after the appearance of system instability, or a failure. Little effort was spent trying to understand the failure mechanism. As a result, signal integrity was jokingly referred to as "black magic," rather than engineering. Third, a very limited number of tools and methodologies were available with which to model the parasitic effects in digital systems accurately. Finally, the roles and responsibilities of SI engineers were not well defined. As stated before, most engineers had diverse technical backgrounds, and most had a primary job other than SI engineering.

Fortunately, researchers working for high-end system manufacturers (such as IBM®, DEC®, HP®, and Bell Labs®) and engineering schools devoted a vast amount of time to modeling and analyzing interconnect systems. Although their work was published in technical journals and conferences (beginning in the early 1970s), there were no textbooks on these topics, as their applications were limited to very high-end computing systems, such as supercomputers and mainframes.

1.1.2 1990–2000: Era of "Passive Channel"

By the early 1990s, the data rates within a computer system had reached several hundred megabits. For example, a high-end PC system had a memory system running at 500–800Mb/s in the early 1990s, while Intel's microprocessor was operating in the gigahertz range. Noise considerations for such systems became much more important. An early signal integrity–related conference called Electrical Performance of Electronic Packaging was established in 1992, and a few other electrical engineering conferences included signal integrity as part of their conference sessions. During this period, SI engineering was quickly developing and rapidly changing in both technical breadth and depth. More practical issues and solutions soon complemented the early research work done by the high-end system manufacturers and university researchers. Figure 1.1 illustrates an SI engineer's various tasks in a typical design process. Many pieces of the "puzzle" had to fit together in order to design a robust high-speed digital system. In contrast to SI engineering in the pre-1990 period, SI engineering was now no longer an afterthought, but an integrated part of high-speed digital system designs. Tools and methodologies that were once only available to a few high-end system manufacturers became readily available through various EDA vendors.

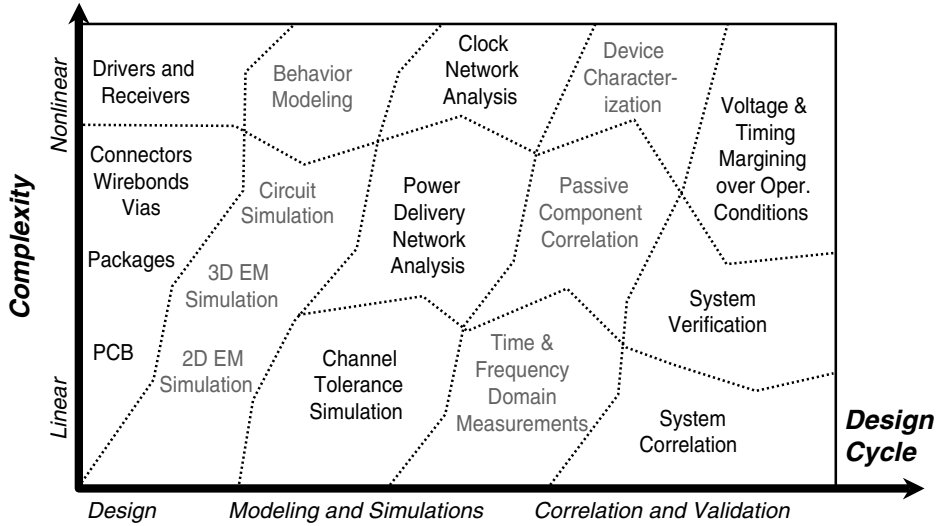

Figure 1.1 SI Engineering Tasks for High-Speed Digital System Design

During this period, much of the SI analysis focused on modeling transmission lines. With HSPICE stable and accurate transmission-line model implementation, engineers were finally able to evaluate the impact of crosstalk, loss, and reflections. Frequency dependent loss, due to dielectric and conductor skin loss, was conveniently evaluated in transient analysis. Electromagnetic (EM) 2D and 3D solvers became available with which to extract either RLGC

(Resistance, inductance, conductance, and capacitance) matrices or scattering parameters. SI engineers created SPICE circuit models based on physical designs using EM modeling. Correlation was performed to validate the passive model in the time domain (using time domain reflectometry [TDR]/scope), or in the frequency domain (using vector network analyzer [VNA]). Finally, the system time and voltage margins under worst-case operating conditions were verified.

Much of the SI work of this period focused on passive-channel modeling and its correlation with hardware measurements. This period can be characterized as "modeling from transmitter die pad to receiver die pad." Everything in the passive channel was modeled. However, what was implemented in silicon was treated as a black box. Behavior models (such as IBIS) were often adopted for transmitter and receivers to minimize SPICE transient simulation time. The interaction between the passive channel and active (Tx/Rx) circuits was ignored, or poorly modeled. Even when a "violation" of the passive channel specification was observed, the overall system failure could not necessarily be concluded. Furthermore, many companies did not understand the importance of signal-integrity engineering; some continued to treat SI as a back-end process, and ignored it until problems appeared later in the design cycle. In addition, there was still some debate regarding the roles and responsibilities of SI engineers, and the future of SI engineering [20]. In summary, SI engineering played an important, but limited, role in high-speed digital system design during the 1990s.

1.1.3 2000–Present: Era of "Entire Link"

At present, data rates for computing systems have reached several gigahertz levels. For example, Sony's PlayStation® 3 uses a differential XDR™ memory system that supports data rates ranging from 3.2Gb/s to 6.4Gb/s. Intel's microprocessor currently operates at more than 3GHz. Data rates for parallel on-board interfaces and high-end graphics memory interfaces have reached several Gb/s levels. Data communications for modern routers and switches have driven the need for very-high-speed serial links. For example, the Optical Internetworking Forum (OIF) standards call for 6 to 12Gb/s for backplane systems. For multi-gigahertz applications, the channel often defines the speed limit. As a result, much of the design attention focuses on mitigating the non-ideal physical effects caused by channel, and in particular, by inter-symbol interference (ISI).

During this period, SI has become one of the important architecture drivers. SI engineers now interact with system architects, circuit designers, and system engineers throughout the design cycle: from conception to mass production to cost reduction. SI engineering has gone beyond conventional passive interconnect modeling, and now attempts to model the entire link. This includes the transmitter, receiver, clock, and channel. SI engineering excels in signaling architecture analysis and performance trade-offs. SI modeling analysis of the entire link influences design issues, such as equalization architecture, clock architecture, timing calibration architecture, coding, and/or error correction architectures. A significant portion of this book is dedicated to this new era of signal integrity analysis, which is henceforth referred to as signaling analysis.

1.1.4 Future: Era of "Power Optimized Link"

This section describes new areas where SI analysis will be required in the near future, based on the authors' current experience and technology trends. Briefly look back at what has happened in the past from a device point of view. The scaling of CMOS feature size and voltage has helped maintain constant power per unit area [21] allowing more transistors to be packed in the same area. This directly increased the performance of the chip, which in turn, required a high-speed I/O interface. However, the voltage scaling has significantly slowed, as the threshold voltage (Vth) could not scale accordingly due to leakage power. As a result, power consumption per unit area is no longer constant and continues to increase. Figure 1.2 shows this scaling trend and the power consumption for microprocessors.

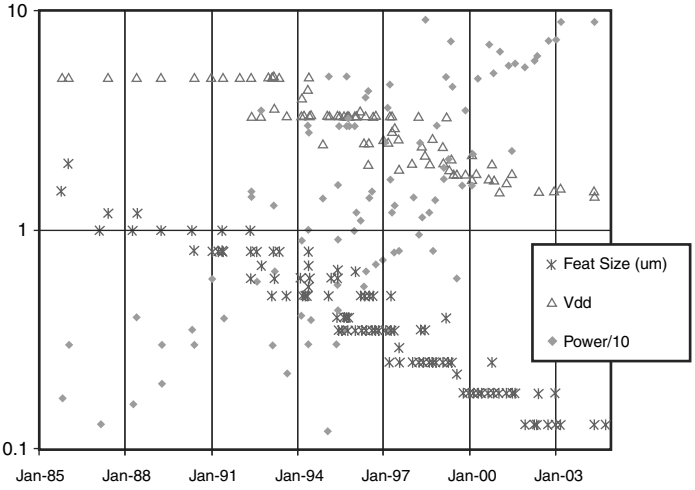

Figure 1.2 Microprocessor Vdd, Power/10, and Feature Size vs. Year [21] (© 2005 IEEE).

Given the slowdown in voltage scaling, the current generation of I/O interface designs needs to consider the optimized data rate for a target process. Power per bit became a common metric for evaluating the link performance, rather than pure performance. Power consumption for a given process is normalized, in terms of FO4 (fan out of 4) delay time, in order to predict the optimum data rate, independent of process technology in [22]. Basic trade-off analysis, in terms of data rate and power consumption with different signal conditioning schemes, would be useful in future signaling analysis.

Traditional I/O interface designs focus on one target data rate, which represents the highest performance in terms of data rate, power consumption, and system cost. This is no longer sufficient for power-critical applications, such as fast-growing mobile applications. Application

processors for such systems now use multiple I/O data rates to optimize the power consumption for various applications. Furthermore, extensive power-managing schemes, such as shutting down the I/O interface (or portions of it), are now commonly employed [23]. Therefore, signaling design must consider a wide range of data rates, and signal integrity analysis must consider non-ideal conditions (due to transitions to different power modes or data rates), to achieve uninterrupted or minimum degradation of I/O performance.

3D integration is another new area to apply signaling analysis. 3D integration shortens the I/O channel, but is subject to more on-chip noise, because the small form-factor makes providing a stable supply quite challenging. In this application, I/O performance is limited more by clock distribution, because the clock tree can span a greater distance than the I/O interconnect itself. Modeling and minimizing the jitter of the clock distribution is crucial in this application. So far, the impact of core noise on I/O has largely been neglected, as I/O typically has a separate power rail (but this may no longer be true for 3D integration). For high-speed I/O with 3D integration, an on-chip power regulator is desirable, and the design trade-off between the on-chip regulator and I/O interface is critical.

On-chip regulators will be more common with off-chip interfaces, because low-swing signaling is desirable for low-power applications [23]. Such interfaces have a minimum output supply noise, even for single-ended signaling designs, and the major supply noise–induced jitter would be from the pre-driver or clock tree. Power supply noise–induced jitter for these circuits will play a more important role, and the signaling analysis must include the impact of these effects. In summary, future signal integrity analysis will be more challenging, and will require a broader knowledge of interface architecture.

1.2 Challenges of High-Speed Signal Integrity Design

This section provides detailed descriptions of a number of the challenges facing signal-integrity (SI) engineers during high-speed SI design.

One challenge is that system-design methodology must change so that SI concerns are accounted for during the architecture phase, rather than later in the process. This issue is more pronounced for designs moving into high data rates. In the past, engineers have relied on their own experience until something goes wrong. This can be very costly in terms of product delay and returns.

SI engineers also need to identify the critical timing and voltage parameters and relationships of the design. Having a good understanding of the signaling methods and clocking architecture is critically important. Not all SI engineers will have the opportunity to work on a new signaling method; most engineers typically work with a standard defined by industry consortium. Even in this case, the SI engineer needs to understand how signaling functions and its key requirements. Identifying worst-case scenarios is also crucial.

SI engineers must be able to build accurate models for passive interconnect as well, including the package, PCB, and connectors. These models must capture frequency dependent loss,

crosstalk, and reflections. They must also capture 3D, as well as full-wave effects. These models can be used in either time-domain or frequency-domain simulations.

SI engineers must build confidence in the accuracy of the passive model by performing detailed correlation with the hardware, in both the time and frequency domains, using VNA and TDR. The impact of manufacturing tolerances must be considered for high volume productions.

SI engineers also need to build an accurate model of the power distribution network, to account for the effects of supply noise on system performance. The power distribution network must not only be appropriate for on-chip power delivery analysis (such as IR, EM, and AC supply noise); it must also be able to capture system behavior, such as coupling between signal and supply rails. The supply voltage tolerance at transistors and package pins must be defined. Bypassing requirements on-chip, on-package, and on PCB must be defined for suppressing high, medium, or low frequency supply noise.

SI engineers need to account for the effects of non-ideal circuit behavior as well, such as transmitter jitter and receiver offset and/or sensitivity. Deterministic noise sources (such as DCD or ISI), and random noise sources (due to thermal or shot noise) must be modeled. The ability of SI engineers to work in a multi-disciplinary environment is very important when accessing the risks or benefits of various design options, and when helping to define an optimal signaling architecture, in terms of both speed and power. Moreover, SI engineers must understand the relationship between supply noise and jitter for a given clocking architecture. Certain clocking architectures may be more susceptible to noise than others. Finding the noise-to-jitter transfer function is essential.

Finally, SI engineers must be able to work in the lab, using various instruments, ranging from VNA, TDR, DCA (digital sampling scope), spectrum analyzers, and BERT (bit error rate tester). One must be able to capture waveforms in the lab, correlate them with simulation, and explain the observed system behavior. Using the correlated model, one must be able to find the root cause of the failure or instability, as well as to recommend design changes for future improvements.

1.3 Organization of This Book

Chapter 2, “High-Speed Signaling Basics,” is an overview of signaling basics. It describes the fundamental blocks of I/O signaling channels and introduces basic I/O interface design. Without delving into details, it depicts an overall description of I/O interface design, including various clocking and topology options that are often not considered in a traditional signal integrity subject. It also covers major noise components in high-speed I/O links. The basic physics of these noise components are discussed, along with modeling issues.

The remaining chapters are organized into four parts. Part I consists of three chapters on passive-channel modeling. The first chapter, Chapter 3, “Channel Modeling and Design Methodology,” presents an overall channel modeling and design methodology. It focuses on a general flow of passive channel modeling. Channel modeling often requires conversion of various network models, and Chapter 4, “Network Parameters,” provides conversion formulae for different

network parameters. It also presents a few issues in S-parameter modeling, which has recently gained more popularity. This chapter also describes the passivity condition of a network parameter. Finally, Chapter 5, "Transmission Lines," discusses the transmission line model, as well as a popular recursive convolution method and its limitations. Generating transmission line models from measurement data is described in detail. The characteristics of three different interconnect types, a PCB trace, package trace, and on-chip interconnect, are discussed.

Part II considers the simulation and analysis aspects of the channel. Five chapters are devoted to this topic. The first chapter, Chapter 6, "Channel Voltage and Timing Budget," discusses challenges in link performance analysis and reviews conventional voltage and timing budget analysis. The remaining four chapters address these challenges, and cover new simulation methodologies. Chapter 7, "Manufacturing Variation Modeling," introduces Design of Experiment (DoE) in channel analysis. DoE guarantees reliable channel performance for mass-production systems with manufacturing variations. Chapter 8, "Link BER Modeling and Simulation," presents a statistical link simulation framework, which can model both device-timing jitter and voltage noise, in addition to the traditional channel effects. Although the statistical link simulator is a powerful tool, used to predict the link's performance, it has a few serious limitations (such as difficulties in modeling non-linear drivers and accounting for data coding). Chapter 9, "Fast Time-Domain Channel Simulation Techniques," explores a fast-time domain simulator, which can be used in conjunction with the statistical framework to mitigate the issues from a pure statistical approach. A significant portion of jitter or noise can be mitigated by using a proper clocking architecture. Chapter 10, "Clock Models in Link BER Analysis," reviews some of the common clocking architectures and their simulation models for statistical link simulators.

Part III explores the impact of power noise to link performance. Chapter 11, "Overview of Power Integrity Engineering," as its name implies, provides an overview of power integrity engineering. Simultaneous Switching Noise (SSN) analysis is a hot issue for modern high-speed memory interface designs. Chapter 12, "SSN Modeling and Simulation," discusses an efficient and accurate simulation methodology for SSN analysis, using a DDR2 memory system to demonstrate the effectiveness of the presented simulation methodology. Noise mechanisms of SSN for common single-ended signaling technologies are also explained. The reduction of SSN is quite challenging, due to the physical limitation of package designs, and Chapter 13, "SSN Reduction Codes and Signaling," presents bus-coding techniques to mitigate SSN. By using differential signaling or data coding, SSN (due to output power supply noise) is no longer the dominant factor for timing jitter. Power supply noise, on the pre-driver and clock path, induces a significant amount of jitter. Chapter 14, "Supply Noise and Jitter Characterization," discusses the basics of power supply noise–induced jitter (PSIJ). Chapter 14 also covers useful on-chip measurement circuits for measuring power noise and power distribution network (PDN) impedance. The proposed measurement technique is further extended to substrate noise measurement in Chapter 15, "Substrate Noise Induced Jitter."

Part IV is devoted to advanced SI/PI topics. Chapter 16, "On-Chip Link Measurement Techniques," describes on-chip measurement techniques for signal performance and noise measurement. Such features are becoming more important, due to the popularity of 3D packages, such as PoP, SiP, and 3D integration. Modern high-speed links utilize signal-conditioning techniques,

used to overcome physical channel limitations, and Chapter 17, "Signal Conditioning," presents a general overview of these equalization techniques. Chapter 18, "Applications," provides three signaling examples to demonstrate the list of common features used in different applications. The first example is an XDR memory system for the high-end PC, game, and graphics applications. Several key architecture-level features, such as FlexPhase for timing adjustment and Dynamic Point-to-Point (DPP) for mitigating multi-drop issues, are also reviewed. The second example is Mobile XDR™ for low-power applications. Additional features, used in Mobile XDR to reduce the interface power, are reviewed in detail. The third example applies these advanced signaling features to the current generation of DDR main memory systems, in order to provide a future roadmap for increasing the data rate. A few highlights of future high-speed interfaces are also presented.

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