Preface

Moore's Law continues to guide the semiconductor technology road map. As the feature size of integrated circuits (ICs) reaches 65 nm today, and moves to 45, 32, and 22 nm in the near future, it will give IC systems more functionality and data-handling capability. A complex and functionality-rich system needs fast input/output (I/O) to be efficient. As a result, we see that the I/O speed keeps increasing as the number of transistors keeps increasing for advanced IC systems.

Although decreasing feature size and increasing I/O speed enable better system capability and performance, they also introduce technological challenges. One of the most important challenges is jitter as I/O speed increases, because the unit interval (UI), the total available jitter budget for a link, must decrease accordingly to ensure a reasonable bit error rate (BER) for a link system. Another very important challenge as the feature size decreases is to constrain the power density and power consumption within limits, implying that low-power design is necessary. As a result, noise becomes a critical challenge, because it needs to be reduced for low-power/low-voltage signals to maintain a reasonable signal-to-noise ratio (SNR). When the same channel material is maintained while the data rate increases, the data signal is attenuated and degraded more due to the same loss channel property and much-increased high-frequency contents associated

with the higher data rate. The signal integrity (SI) due to signal attenuation and degradation is manifested by deterministic jitter and noise. Jitter, noise, and SI challenges get magnified when I/O link data rate increase is achieved by using the same channel material, a common approach used by most of the high-speed I/O standards for cost-effective considerations.

Today, most high-speed I/Os are designed around 5 to 6 Gbps rates for computer-centric applications where copper-based channels are used the most, including standards such as PCI Express II (5 Gbps), Serial ATA III (6 Gbps), and FB DIMM I (3.2, 4.0, and 4.8 Gbps). The next generation of those standards will likely double in data rate and will be at 8 to 12 Gbps rates. For network-centric applications, most current designs are at 8 to 10 Gbps rates, such as Fibre Channel 8X (8.5 Gbps), Gigabit Ethernet (GBE) 10 X (10 Gbps), and SONET OC-192 (10 Gbps), where optical fiber-based channels are used the most. The next generation of network I/O link will likely double or quadruple to 17 to 40 Gbps. At 10 Gbps, the UI is 100 ps, and at 40 Gbps, the UI is only 25 ps. To maintain a good BER (10^{-12}), the random jitter in I/O links at those data rates has to be in sub-ps or less, and that is a very daunting and challenging task. It is conceivable that, in the future, the jitter, noise, and SI challenges will become even harder at higher data rates.

In the past 20 years or so, many books have been published on signal integrity. However, the coverage of jitter, noise, and BER is rather brief and narrow in those books. Only two books have been dedicated to jitter, but that was 15 to 17 years ago, and the contents are outdated in comparison with the today's knowledge and understanding of jitter, noise, and SI.

Significant progress had created new theories and algorithms for in jitter, noise, and signal integrity in the past ten years. As far as jitter theorems and analysis, jitter components such as deterministic jitter (DJ) and random jitter (RJ) and associated math models have been developed as a better metric for jitter quantification. On the jitter-tracking part, jitter transfer function has been used extensively to determine outputs and tolerances for jitter, noise, and signaling quantitatively. Statistical signal analysis methods based on probability density function (PDF), cumulative distribution function (CDF), and the corresponding convolution operation are replacing the conventional simple, unsophisticated, and less accurate peak-to-peak and RMS metrics. Linear time-invariant (LTI) theorems are used regularly, coupling with the statistical signaling and circuit theorems, to determine jitter, noise, and signaling performance for both the link system and the subsystems within it.

At the same time, significant advancements also happened in high-speed networks and computer I/O links in terms of architectures and data rate speed. In general, the architectures developed in those standards are all serial at multiple

Gbps, with its clock timing being extracted at the receiver side by a clock recovery circuit (CRC). The CRC also tracks and reduces low-frequency jitter at the receiver input to maintain a good overall BER performance for the receiver or system. Various clock and data recovery methods and circuits have been developed, including ones based on phase-locked loop (PLL), phase interpolator (PI), and oversampling (OS). Each clock recovery implies a different jitter transfer function and tracking capability and characteristics. To mitigate or compensate for signal degradation due to the lossy channel, extensive and advanced equalization techniques and circuits have been developed, including linear equalization (LE) and decision feedback equalization (DFE). Accordingly, new theorems, algorithms, designs, and test methods have been developed to accommodate the emerging challenges imposed by new architectures, data rates, clock recovery, and equalization for the latest multiple-Gbps high-speed I/O links.

Innovations and breakthroughs have been developed in the past ten years, including theory, algorithm, methodologies for understanding, modeling, and analyzing jitter, noise, and SI. Link architectures, theory, algorithm, and circuits for mitigating them also have been developed. However, no book has focused on all the latest advancements in jitter, noise, and SI in a systematic and cohesive manner. This book was written to fill in this gap.

This book intends to give a concurrent, comprehensive, systematic, and in-depth review and discussion of fundamentals of, new theories about, and algorithms on jitter, noise, and SI, as well as their modeling, testing, and analysis methodologies within the contexts of clock and I/O link signaling. This book covers important topics such as jitter and noise separation theories and algorithms; jitter transfer functions for output and tolerance; clock and PLL jitter; and modeling, analysis, and testing for the link system, covering its subsystems of transmitter, receiver, channel, reference clock, and PLL, with emphasis on jitter, noise, and SI aspects.

We start Chapter 1 with overview of the basics on jitter, noise, and SI and communication link systems. The root cause mechanisms for various jitter, noise, and SI are discussed and the statistical handling for jitter and noise are introduced. Then, we progress to the discussion on jitter and noise components concept and definition and the rationales on why they are necessary and important. In conclusion, we bring the jitter, and noise, and SI discussion to the framework of a communication system.

With a big picture introduction on jitter, noise, SI, and link communication system in Chapter 1, we will dive into the details on the necessary and relevant mathematical in Chapter 2. Theories on relevant statistics, stochastic processes for jitter, noise, and SI, and linear time invariant (LTI) theory for link systems and signaling, and the theory for combining statistics with LTI are introduced in this chapter.

In Chapters 3 and 4, we apply the statistical and stochastic theory introduced in Chapter 2 to quantify jitter, noise, SI, and BER in terms of appropriate PDF and CDF, as well spectrum function of power spectrum density (PSD). In Chapter 3, we give quantitative description for each jitter or noise component in terms of PDF and PSD, along with the relationship between component PDFs to the total PDF, and component PSDs to the total PSD. In Chapter 4, we discuss jitter and noise jointly in a two-dimensional (2-D) frame. The mathematical representations for the joint PDF of jitter and noise (e.g., eye-contour), and joint jitter and noise CDF (e.g., BER contour) are presented.

Chapters 5 and 6 are dedicated to jitter and noise separation to various layers of components. In Chapter 5, we present the jitter separation to its components of deterministic jitter (DJ) and random jitter (RJ) based on jitter PDF or CDF function using the widely used Tailfit method. In Chapter 6, we introduce jitter separation based on real-time function or autocorrelation function of jitter to its first and second layer jitter components of data dependent jitter (DDJ), duty-cycle distortion (DCD), inter-symbol interference (ISI), periodic jitter (PJ), bounded uncorrelated jitter (BUJ), and RJ. Jitter spectrum or PSD estimation via Fourier transformation (FT) is introduced. Both time and frequency domain separation techniques are presented.

With the fundamental knowledge on statistical jitter, noise, and SI, as well as theories and algorithms for construct the total jitter or noise PDF or PSD to total PDF or PSD, or separating total jitter or noise PDF or PSD to its component PDF or PSD, we are ready to solve the practical problems. At high frequencies, clock and PLL jitter become the major limiting factor for their performance and we will dedicate the first application to jitter in clocks and PLLs. Chapter 7 focuses on clock jitter. We start with clock jitter definition and reveal its impacts to both synchronous and asynchronous systems. Next, we introduce three different jitter types of phase jitter, period jitter, and cycle-to-cycle jitter, along with their physical meanings, usage model, and interrelationship in both time and frequency domain. In the end, we discuss the relationship and mapping math models between phase jitter and phase noise, a conventional metric for the performance of a clock or PLL in frequency domain that is widely used in microwave and radio frequency (RF) fields. Chapter 8 is dedicated to jitter and noise in PLLs. First, LTI model for PLL in both time and frequency domain are introduced, along with functional and parametric analysis methods. Second, generic jitter and noise analysis and modeling methods are introduced using autocorrelation function in time domain and PSD function in frequency domain. Third, comprehensive and detailed modeling and analysis are presented for jitter, noise, and transfer functions for both 2^{nd} and 3^{rd} order PLLs.

Chapters 9, 10, and 11 are dedicated to the jitter, noise, and SI in a high-speed link, covering three important aspects of physical mechanisms, modeling

and simulation methods, and test and verification methods. Chapter 9 focuses on jitter, noise, and SI physical mechanisms for the purpose of establishing a good understanding. Subsystem architecture including transmitter, receiver, channel, and reference clock and physical mechanisms for jitter, noise, and SI within each are presented. Chapter 10 devotes to quantitative modeling and analysis for high-speed link system and its subsystems. Modeling methods based on LTI theorem are developed for the subsystems and the entire system through LTI cascading. Subsystem models of jitter, noise, and signaling for transmitter, receiver, and channel are presented. Importance elements of equalization and clock recovery are included in the modeling. Both linear and DFE equalizations are covered. Chapter 11 dedicates to testing and analysis for the high-speed link system and its subsystems. Testing requirements and methods for link subsystems of transmitter, receiver, channel, reference clock, and PLL are presented. Latest testing methods of reference receiver that is composed of both reference clock recovery and equalization for jitter, noise, and signaling output, as well as worst case jitter, noise, and signaling generation methods for receiver tolerance testing are presented. At the end of this chapter, link system level test method such as loopback is introduced and trade-offs between on-chip built-in-self-test (BIST) and off-chip external test is discussed.

Chapter 12 gives the summary of the book, discusses the trend, outlook, and challenges for jitter, noise, and SI in the future.

This book is written for readers such as engineers and managers working on high-speed circuits, devices, and systems for industry. A wide range of engineers can benefit from reading this book, including design engineers, test engineers, application engineers, and system engineers who are already in or about to enter the field of jitter, noise, signal integrity, and high-speed links. It is also written for researchers, professors, and students who are either in this field or plan to enter it. This book aims to give you a comprehensive understanding of jitter, noise, and signal integrity, as well as high-speed link signaling and performance.